ACCELERCOMM
SUPERCHARGED WIRELESS

LDPC for high performance applications

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Advanced channel coding solutions for high performance communications systems

LDPC FOR HIGH PERFORMANCE APPLICATIONS

Today's high performance communications systems, such as 3GPP 5G New Radio (5G NR) and the latest Low Earth Orbit (LEO) satellite systems, make use of Low Density Parity Check (LDPC) codes to encode information to protect it from errors during transmission in a process often referred to as Forward Error Correction.

AccelerComm's advanced channel coding solutions achieve market leading performance in terms of error rates and efficiency to maximise overall system performance.

MAXIMIZING SYSTEM PERFORMANCE

LDPC decoding is a complex, resource intensive process, and the performance of the decoder has a profound impact on the overall system performance. An optimized decoder will be able to correctly recover the data from transmissions with a higher signal to noise ratio (SNR) than a non-optimized decoder can achieve.

By optimizing the decoder and supporting functions it is possible to realise benefits up to 1dB which when translated into system performance represent a 20% increase in capacity, or a 20% reduction in radiated power. With convergence between satellite and 3GPP standards AccelerComm™ has developed advanced flexible solutions that can be optimized for a range of high performance applications, and is engaged in advanced research to bring learning from the latest academic studies to implementations with even greater benefits.

20% less power

OR

1.2 x capacity

50% less power

OR

2 x capacity

OPTIMIZED FOR HIGH PERFORMANCE COMMUNICATIONS

AccelerComm's LDPC decoding IP is specifically designed for use in high performance communications systems, it has a number of features not found in generic decoders designed for lower performance use cases.

DESIGNED FOR 3GPP STYLE CODES

In adopting the use of LDPC codes 3GPP has specified their use in an innovative way that maximizes flexibility whilst maintaining performance. Unlike many generic LDPC codecs the AccelerComm™ solution is designed from the ground up for the 3GPP approach and fully exploits the flexibility and performance inherent in the design.

ADVANCED ALGORITHMS

The algorithm used by the IP can be selected to match the requirements of specific use cases, delivering gains of up to 0.4dB compared with some fixed algorithms.

MINIMIZE ERROR FLOORS

The IP can be configured to almost completely avoid a condition known as error floors that can cause retransmissions and present a particular challenge to satellite applications and ultra-reliable terrestrial application.

SOFT DECISION OUT

The IP includes the option of a Soft Decision output for use in more accurate link quality measurements and techniques such as successive interference cancellation.

FLEXIBLE TARGETS

Designed to be deployed in a range of targets, such as FPGA, ASIC or a pure software implementation.

CLASS LEADING EFFICIENCY

The design consumes up to 40% less area and up to 50% less power per bit than competing solutions. LDPC decoding is typically a significant component within a digital modem and so these savings have a major impact on overall resource and power consumption.

EXTENSIVE DESIGN SUPPORT

A full suite of reference kits and design support tools such as test benches is provided to reduce integration time and cost.

ADAPTABLE TO A WIDE RANGE OF USE CASES

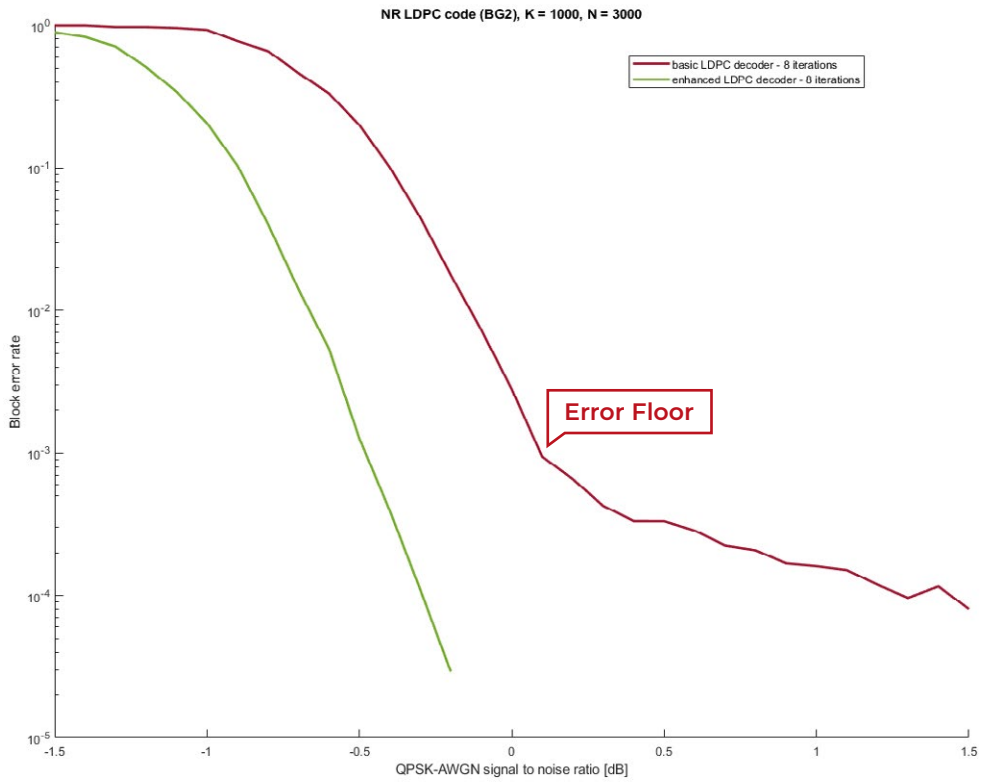
LDPC decoder design is a compromise between many factors and in high performance applications the compromises must be finely tuned to deliver maximum system performance. There are several algorithms in common use for LDPC decoding each with different characteristics, for example in satellite applications achieving the highest level of error correction to avoid costly retransmissions may be more important than delivering low latency in the decoder, whereas in terrestrial cellular systems higher throughputs may be required but retransmissions carry less penalty. AccelerComm™ support a range of algorithms including normalized min sum, adaptive normalized min sum and offset min sum with optimizations, to allow the best options to be chosen to suit the application.

As well as algorithm choice there are many other design time options such as flexible parallelism. Parallelism occurs at several levels within the decoder and all of these can be selected to optimize the overall solution. By choosing the correct parallelism to match the characteristics of the radio frame structure, and the expected number of simultaneous users, pipelining can be increased, leading to savings in memory needs and increased throughput. Factors such as LLR width and internal pipelining depth can be further tuned to match the decoder to the system requirements as closely as possible.

Parameter	Options	Impact
Algorithm variant	10 options	Trade off between performance at high and low BLER rates and area
Parallelism	Independently scaled	Trade off between throughput and latency against area
Pipeline depth	Tuneable	Optimized to match fmax and throughput of target
LLR Width	5 or 6 bits	Works with algorithm variant to optimize performance
Optional features	HARQ, Soft Out, DRAM width	Configure to match application

NO ERROR FLOORS – CRITICAL FOR SATELLITE APPLICATIONS

The term error floor is used to refer to a tail off in performance of an LDPC decoder at low error rates. It is a feature of almost all decoders, a point is reached where improving the SNR leads to a reduced rate of improvement in error rate leading to a small number of residual errors. Terrestrial cellular systems use an efficient system of resending data referred to as HARQ to deal with uncorrected errors. 5G NR is increasingly being targeted at industrial and other critical applications requiring high reliability and low latency, referred to a URLLC applications, and in these applications HARQ retransmissions must be reduced to a minimum. In a satellite system with limited bandwidth and long transmission latencies HARQ must be reduced even further. AccelerComm's LDPC decoder can be configured to significantly reduce error floors, reaching Block Error Rates (BLER) below 1 x 10-6. By use of an LDPC decoder with extremely low error floors the occurrence of HARQ can be greatly reduced allowing high reliability links to be realized without resorting to higher coding rates and low modulations schemes, maximizing spectral efficiency in critical applications.



CELLULAR USE CASE

As an example of a terrestrial cellular 5G use case, 8 parallel instances of the decoder, each of which has an internal parallelism of 8, can be configured to accommodate a peak throughput of 20Gbps with a processing time of under 15 microseconds, suitable for all but the most extreme low latency use cases. Compared to a typical competitor this configuration delivers 0.4dB improvement in BLER (i.e it can deliver the same BLER with a SNR 0.4dB worse), 81% increase in throughput for a given FPGA resource and 56% reduction in energy per bit. The processing time, which directly impacts latency, is already 27% lower than the typical competition but could be configured to be lower still at the expense of other parameters for use in specialist base stations targeted at the most extreme URLLC applications.

Performance comparison to leading competitor

<0.4dB
Improvement in BLER

27%
Reduction in latency

81%
Increase in throughput per kLUT

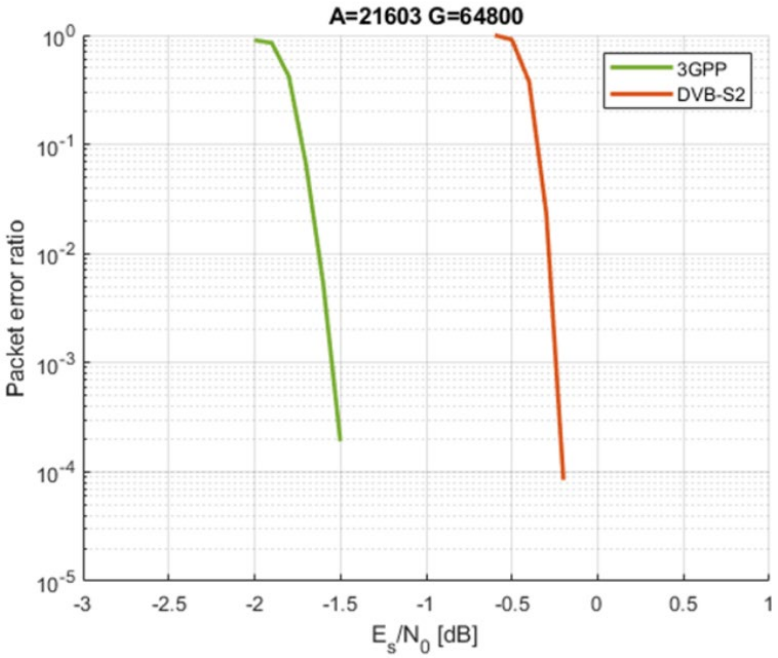
56%
Reduction in energy per bit

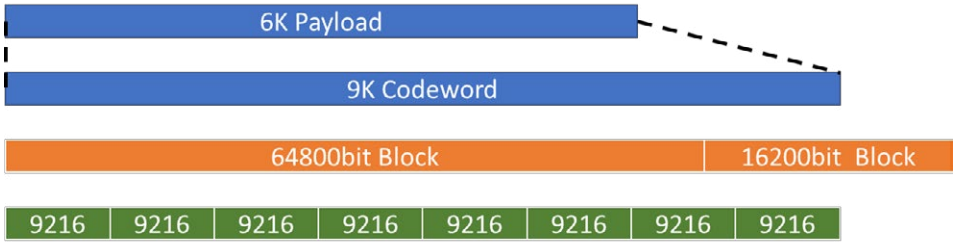
SATELLITE BROADBAND USE CASE

Several operators planning to use Low Earth Orbit satellite systems are considering the use of 3GPP LDPC codes as an alternative to DVB-S2X codes typically used in satellite broadcast applications.

DVB-S2X has far less flexibility than the 3GPP code which, whilst not a limitation for broadcast applications, has performance impacts with the smaller payloads typical of broadband internet traffic. Rate matching to the nearest block size can lead to performance loss of up to 1dB or wasted spectrum.

DVB-S2X uses a second code to prevent error floors and this code restricts flexibility. By providing an implementation of the 3GPP codes that can avoid error floors down to Block Error rates of less than 1 x 10-6 without the uses of a second code, AccelerComm™ enables the flexibility of 3GPP codes to be used in satellite applications with no sacrifice in performance or spectral efficiency.





ADVANCING WIRELESS COMMUNICATION

AccelerComm™ is at the forefront of bringing the latest academic research on theoretical techniques such as using decoder feedback in the equalizer to reality, with practical solutions that can operate at the throughputs required for high performance communication systems. AccelerComm™ has developed novel techniques to overcome the significant implementation challenges these advanced techniques present and plans to deliver solutions which will bring major system performance improvements as well as capacity and efficiency gains.

For more information visit us at
www.accelercomm.com

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AccelerComm™ is a semiconductor IP-core company that provides patented channel coding solutions. Our team has a proven track-record of channel coding and IP expertise, from developing and optimizing algorithms through to their implementation and delivery in FPGA and ASIC architectures. With more than 100 published IEEE papers and numerous citations for our work in 3GPP RAN1, we are having a significant impact on the mobile communications world.

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