ACCELERCOMM
SUPERCHARGED WIRELESS

5G PDSCH Encoder, PUSCH Decoder Product Overview

July 2021

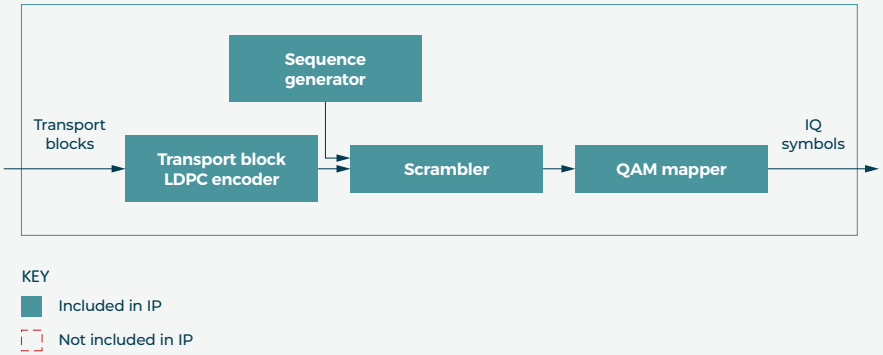
3GPP compliant coding and modulation for 5G NR Physical Shared Channels

INTRODUCTION

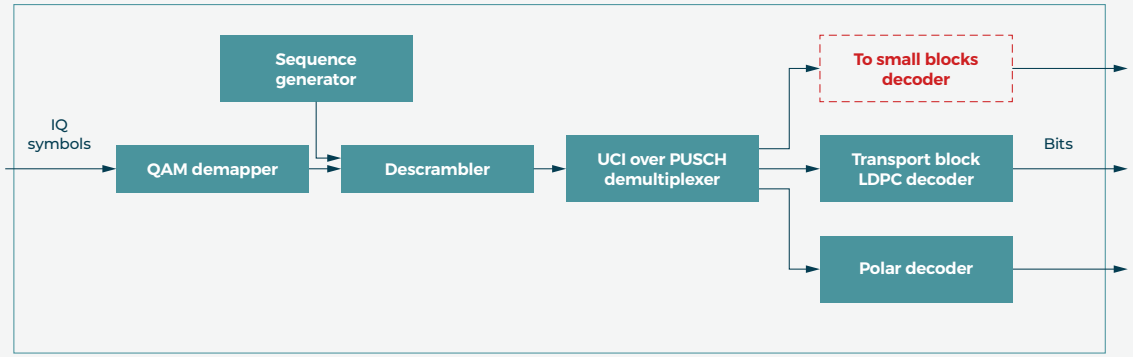
AccelerComm's latest QAM modulator and demodulator complements our existing LDPC and Polar encoding and decoding solutions to create a complete high performance 3GPP compliant PDSCH encoder and PUSCH decoder for a gNB.

INTRODUCTION

PDSCH Encoder



PUSCH Decoder



5G NR introduces the use of 256QAM modulation for the downlink and uplink physical shared channels (PDSCH and PUSCH). It also allows for Uplink Control information (UCI) to be multiplexed onto the PUSCH as per TS 38.212 sec 6.3.2, complicating the uplink demodulator design. Whilst the specification is designed so that a simple demodulator will function, it includes opportunities to improve the detection of some key control messages.

The AccelerComm™ Demodulator component fully exploits the opportunities provided in the specifications to deliver the lowest possible error rates for the UCI messages, improving capacity and reducing latency.

Integrating and validating the many functional blocks of the physical layer consumes significant engineering resource and by providing a complete pre integrated IP solution, AccelerComm™ greatly simplifies the design of a high performance gNB.
For instance, a key bottleneck in the Uplink receive chain is often the very high data rate required to pass data to the LDPC decoder as LLRs. By integrating the Demodulator and LDPC Decoder and passing the data as IQ values, the AccelerComm™ IP offers an opportunity to reduce this bottleneck by a factor of two.

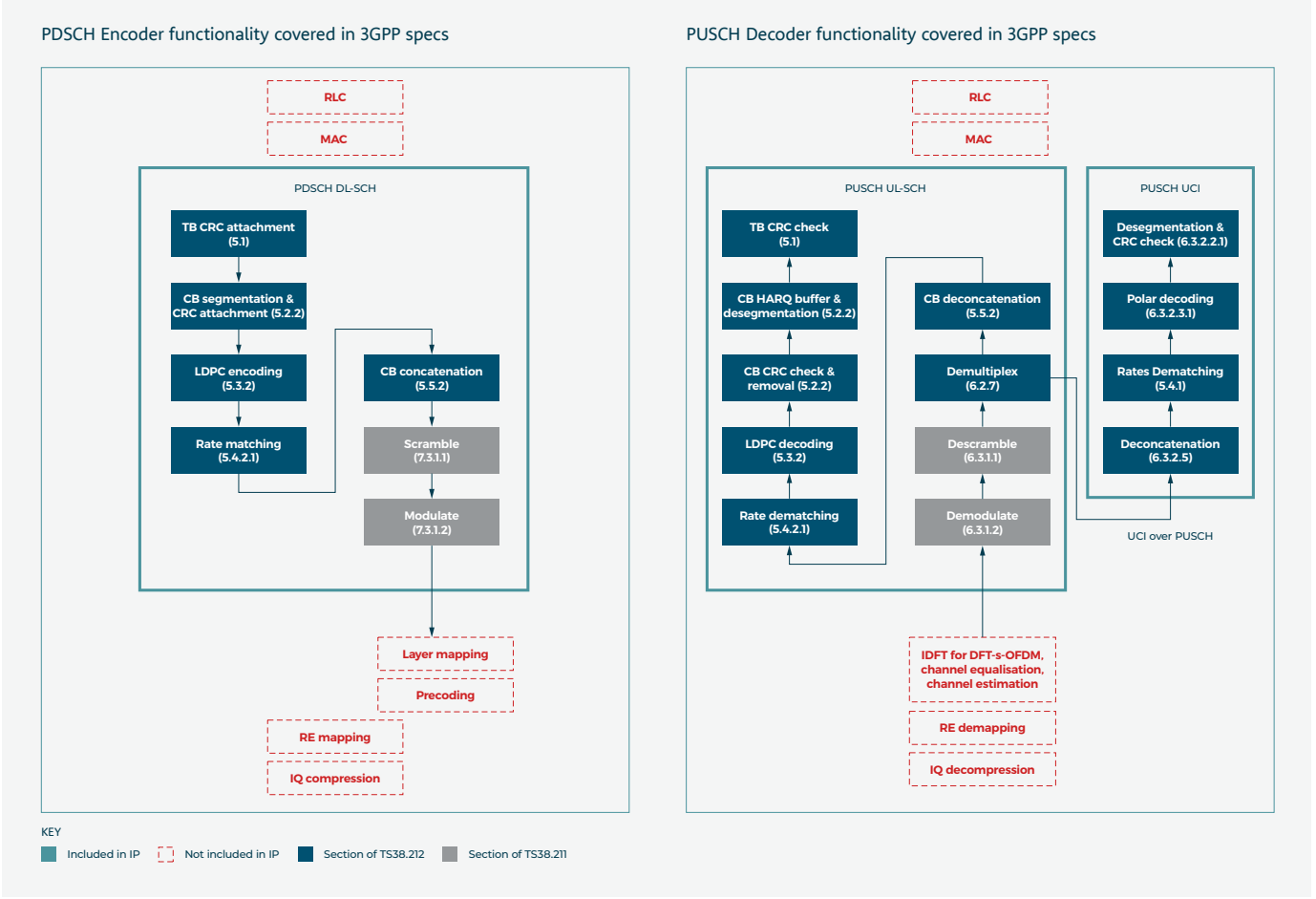
FUNCTIONALITY

The AccelerComm™ PUSCH Decoder and PDSCH Encoder products provide complete functionality for both uplink and downlink processing in a gNB covering the relevant sections of TS 38.211 and 38.212.

PDSCH Encoder features the new QAM mapper and Scrambler functionality. These are integrated with LDPC encoder and transport block chain components.

PDSCH Decoder features the new QAM demapper, descrambler and demultiplexer. These new functions are integrated with LDPC and Polar decoders and transport block chain components.

PUSCH Decoder also allows for Uplink Control information (UCI) to be multiplexed onto the PUSCH. Complete integration of the relatively complex demultiplexer is tightly integrated which not only simplifies development for the end user but also leads to improved multiplexed UCI BLER for critical HARQ-ACK messages.



BENEFITS AND PERFORMANCE

The AccelerComm™ PDSCH Encoder and PUSCH Decoder products simplify the creation of high performance 5G NR implementations.

- Complete implementation of the relevant 3GPP standards
- Improved BLER, especially for UCI control data
- Pre integrated with AccelerComm™ LDPC and Polar encoder/decoder chains and inherits all the benefits from these
- Single control interface
- Supported across FPGA and ASIC platforms
- Highly configurable for a wide range of base station (gNB) applications
- Configurable to support maximum throughputs and minimum timing requirements for all numerologies
- Very low latency – meets strictest requirements for uRLLC
- Efficient design – saves device area
- Easy to integrate using industry standard AXI interfaces

5G NR targets throughputs up to 20Gbps with sub 1ms latencies, across a wide range of radio conditions, however the standard is flexible, and many applications require lower performance targets. Like all AccelerComm™ IP the PUSCH Decoder and PDSCH Encoder is configurable to several different parallelisms to optimise the area / power / performance of each solution.

Throughput between functional blocks is often a design challenge, especially in a software system using hardware acceleration. The input of the demodulator is represented by IQ values. At high Modulation Coding Rates (MCR) the IQ representation is more compact than the LLRs used as the input to the LDPC decoder representing a reduction of up to 2X in interconnect bandwidth needed when the demodulator and decoder are separate functions.

In many systems the LDPC accelerator is accessed over a PCIe interface, and this can be a bottleneck, moving the demodulator to the accelerator potentially doubles the capacity of the PCIe interface.

IMPROVED MULTIPLEXED UCI BLER

When sending short ACK messages over the UCI channel multiplexed over PUSCH the standard specifies the use of placeholder filler bits which maximise the chances of correctly decoding these critical messages. As the AccelerComm™ QAM demapper is integrated with the demultiplexer, it can identify the QAM symbols that represent the ACK bits and process them, accordingly, ensuring the lowest possible error rate.

COMPLETE DECODER INTEGRATION

The new modulator and demodulator components are available in complete integrated IP packages with AccelerComm's high performance LDPC and Polar encoders and decoders. This integration simplifies development, for example the Polar and LDPC encoder/ decoder and modulator / demodulator require several control parameters for each transport block sent over the PxSCH, the integrated IP block brings all the relevant information together into a single control interface.

DESIGN SUPPORT

AccelerComm™ provide industry leading support for the core IP product suite including a full test bench to prove 3GPP conformance that can be used in the most popular simulation tools, Mentor ModelSim or Questa and Cadence Xcelium, and a bit accurate C model is also included for use in user simulations or in MATLAB.

AccelerComm™ provides support services to customers to help them with the integration of the IP into their designs, but typically this is a very straightforward process.

Our flexible IP can be configured to closely match the requirements of a wide range of designs, and then the combination of simple interfaces, complete documentation and supporting test harnesses and reference kits, backed up by our experienced support team mean that IP can be integrated and running within a day.

For more information visit us at
www.accelercomm.com

AccelerComm™ is a semiconductor IP-core company that provides patented channel coding solutions. Our team has a proven track-record of channel coding and IP expertise, from developing and optimizing algorithms through to their implementation and delivery in FPGA and ASIC architectures. With more than 100 published IEEE papers and numerous citations for our work in 3GPP RAN1, we are having a significant impact on the mobile communications world.

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