SYNOPSYS®

DesignWare Processor IP Portfolio

- Scalable family of 32-bit and 64-bit processors, wide-vector processors, vision processors, and subsystems
- Maximum power and area efficiency (DMIPS/mW, DMIPS/mm^2) for embedded applications
- Highly configurable so each instance can be optimized
- Extensible instruction set enables application-specific customizations
- Integrated tool suite with broad hardware and software ecosystem support

DesignWare Processor IP Portfolio

EM Family Ultra-low power embedded processing	SEM Family Security processors for embedded applications	HS Family High-performance control	VPX Family High-performance digital signal processing	EV Family AI-enabled embedded vision
· Optimized for ultra-low power · 3-stage pipeline RISC processors with RISC + DSP · Maximum performance and area-efficiency: up to 1.81 DMIPS/MHz and as small as 0.01mm^2	· Power- and area-efficient security processors for IoT and mobile applications · Protection against hardware, software and side channel attacks · SecureShield for Trusted Execution Environments	· Highest performance ARC cores · 32-bit and 64-bit processors · Single or dual issue · High-speed 10-stage pipeline, SMP Linux support · Single- and multicore configurations up to 12 cores	· VLIW/SIMD architecture for highly parallel processing · Multiple vector floating point engines · Acceleration for linear algebra and complex math functions · Optimized MLI running on DSP processor	· Multicore design optimized for vision processing · High-performance vision engine can be configured for 8-, 16-, or 32-bit operations · Programmable deep neural network engine

Functional Safety Processor Portfolio
· Support for ARC EM, EV, HS, SEM and VPX Processor Families
· Integrated hardware safety features to detect system errors
· Acceleration of ISO 26262 certification for safety-critical automotive SoCs

Processor IP

Synopsys' processor IP portfolio includes the DesignWare® ARC® processors and subsystems, software, development systems and tools. ARC processor cores are based on a flexible and proven 32-bit instruction set architecture (ISA) with features optimized for a broad range of embedded and deeply embedded applications:

- Performance-efficient designs deliver maximum performance while consuming a minimum amount of power and silicon area
- Highly configurable processors can be performance- and power-optimized for each instance on an SoC while sharing a common programming model
- Extensible ISA supports user-defined custom instructions, enabling integration of users' proprietary hardware to accelerate application-specific tasks
- Streamlined system integration through the ability to closely couple memory and directly map peripherals to the core, reducing system latency and cost

ARC EM Processors

The ARC EM Family includes the ARCv2 ISA-based ARC EM4 and EM6 as well as the DSP-enhanced EM5D, EM7D, EM9D and EM11D. The ARC EM4, EM5D and EM9D processors support instruction and data CCMs and the EM6, EM7D and EM11D additionally support instruction and data caches. The EM9D and EM11D feature support for XY memories to deliver higher levels of signal processing efficiency. The ultra-compact EM cores feature excellent code density, small size and very low power consumption, making them ideal for power-critical and area-sensitive embedded and deeply embedded applications.

Along with optional FPU, MPU, µDMA, Real-Time Trace and ARConnect for multicore integration, the EM Family also offers an Enhanced Security Package , which provides tamper protection features and enables designers to create a trusted execution environment that protects their systems and software from evolving security threats such as IP theft and intentional remote attacks.

In addition, the CryptoPack option for EM cores uses ARC Processor EXtension (APEX) technology to accelerate common cryptographic software algorithms.

ARC SEM Security Processors

The ARC SEM Family includes the ARCv2 ISA-based ARC SEM110 and SEM120D security processors to protect against logical, hardware and physical attacks. The SEM processors include SecureShield™ technology with a secure MPU that enables the creation of a Trusted Execution Environment (TEE) to protect secure functions from software vulnerabilities that may exist in user code. The ARC SEM110 is a 32-bit RISC core that is optimized for performance, power, and area efficiency. The ARC SEM120D has an added DSP instruction set and unified multiply/ MAC unit. The ARC CryptoPack, FPU and µDMA licensable options are available for the ARC SEM processors.

The ASIL D compliant DesignWare ARC SEM130FS Safe and Secure Processor simplifies development of safety-critical automotive applications while enabling designers to integrate security into their SoC to protect against logical, hardware and physical attacks. The ARC SEM130FS processor is supported by a comprehensive set of safety work products and the ARC MetaWare Toolkit for Safety with ASIL D Ready certified compiler to generate ISO 26262 compliant code..

ARC HS Processors

The ARC HS Family includes the ARC HS56, HS57D, HS58, HS66, and HS66, which are based on the new ARCv3 instruction set architecture (ISA), and the ARCv2 ISA based HS34, HS36, HS38, HS44, HS46, HS48, HS45D and HS47D processors.

All HS processors support closely coupled memories (CCMs), which enable single-cycle access to instructions and data. The HS family processors (except HS34, HS44 and HS45D) add up to 64 KB each of instruction and data caches. The HS38, HS48, HS58, and HS68 also include an advanced memory management unit (MMU) to support Linux and other high-end operating systems.

The ARC HS4x, HS5x, and HS6x processors feature a high-speed 10-stage, dual-issue pipeline that supports out-of-order execution. The HS45D, HS47D, and HS57D support more than 150 DSP-optimized instructions, delivering a unique combination of high-performance control and high-efficiency digital signal processing. The processors are compatible with the ultra-low power ARC EMxD processors and have the same instruction set, making it easy to migrate code between the two processor families. HS processors are optimized for GHz+ operating speeds with minimum area and power consumption, making them ideally suited for embedded applications with very high-performance requirements. The HS3x and HS4x processors are available in single-core, dual-core, and quad-core configurations, and the HS5x and HS6x are available in single-core and multicore configurations with support for up to 12 cores.

ARCv1 ISA-Based Processor Families

The ARC 600, ARC 700 and AS2xx processor families are based on the ARCv1 ISA. The ARC 600 and ARC 700 product lines are general purpose processor cores extensively deployed in high-volume production. Target applications range from deeply embedded control to DSP-intensive processing and Linux host. The ARC AS200 Family includes the AS211SFX and AS221BD audio processors. These processors feature powerful audio processing capabilities and support a broad portfolio of certified audio codecs and post-processing software from a range of popular standards including Dolby®, DTS® and Microsoft®.

ARC Processor EXtension (APEX) Technology

ARC processors support the addition of user-defined extensions to the core. These extensions can take the form of more processor and auxiliary registers, new instructions, and/or additional condition code tests. Custom instructions enable designers to efficiently add their proprietary hardware to the processor to further increase application performance.

ARC VPX DSP Processors

The ARC VPX DSP Family includes the ARC VPX2, VPX3 and VPX5 processors, which are based on an extended ARCv2DSP instruction set architecture and optimized for a broad range of high- performance signal processing applications such as IoT sensor fusion, natural language processing, RADAR/LiDAR, and baseband communications processing. The VPX DSPs implement a configurable, energy-efficient very long instruction word (VLIW)/ single instruction-multiple data (SIMD) architecture that combines scalar and vector execution units to enable a high degree of parallel processing. The VPX2 and VPX3 DSPs are available in single- and dual-core configurations and support 128-bit and 256-bit vector word lengths, respectively. VPX5 is available in single-, dual-, and quad-core configurations and supports 256-bit vector word lengths. To speed application software development, the VPX family is supported by Synopsys' ARC MetaWare Development Toolkit, which provides a comprehensive and vector length-agnostic software programming environment that enables code portability among all members of the VPX family. The tool suite includes an optimizing C/ C++ vector compiler, debugger, instruction set simulator, as well as DSP, machine learning inference and math libraries.

Embedded Vision Processors

The ARC EV7x Embedded Vision processors are fully programmable and configurable IP cores that have been optimized for artificial intelligence and deep learning applications, combining the flexibility of software solutions with the low cost and low power consumption of hardware. The EV7x Processors integrate scalar, vector DSP and deep neural network (DNN) processing units for highly accurate and fast vision processing. The ARC EV7x Vision Processors integrate up to four enhanced vector processing units (VPUs) and a DNN accelerator with up to 3,520 MACs.

The EV Processors are designed to integrate seamlessly into an SoC and can be used with any host processors and operate in parallel with the host. With up to four vector DSPs that operate in parallel to the DNN engine, the EV7x Processors provide scalable performance that supports convolutional neural network (CNN) and recurrent neural network (RNN) graphs. In addition, an optional IEEE 754-compliant vector floating point unit, integrated into the vector DSP core, and its supporting software, offer performance levels of up to 328 Gigaflops for single precision operations and 655 Gigaflops for half precision operations. The embedded deep neural network engine accelerates the processing of CNN/RNN executables, enabling accurate and power-efficient object detection, image classification, and convolutional LSTMs.

ARC Functional Safety Processors

The DesignWare ARC functional safety (FS) processors support ASIL B and ASIL D safety levels to simplify safety-critical automotive SoC development and accelerate ISO 26262 qualification. The portfolio includes the ARC EM22FS, EV7xFS, HS4xFS, SEM130FS, and VPXxFS VPXxFS safety processors with integrated hardware safety features such as redundant processors, error-correcting code (ECC), parity protection, safety monitors, and user-programmable windowed watchdog timers to detect system errors. The DesignWare ARC MetaWare Development Toolkit for Safety (EM22FS, HS4xFS, SEM130FS, VPXxFS) and MetaWare EV Development Toolkit for Safety (EV7xFS) help software developers accelerate the development of ISO 26262-compliant code.

ARC Processor Subsystems

ARC IoT Communications IP Subsystem

The DesignWare ARC IoT Communications IP Subsystem is an integrated, pre-verified software defined modem that adapts to continuously evolving standards. It integrates an ARC EM11D processor, tightly coupled memories, hardware accelerators, dedicated peripherals and software libraries to deliver efficient real-time control and DSP performance for IoT applications requiring low bandwidth wireless communication.

ARC Data Fusion IP Subsystem

The DesignWare ARC Data Fusion IP Subsystem is a complete, pre-verified, hardware and software solution optimized for a wide range of ultra-low power IoT applications. It is designed for fast and easy integration within a larger system context. The fully configurable ARC Data Fusion IP Subsystem includes the choice of a low gate count and energy-efficient ARC EM5D, EM7D, EM9D or EM11D processor for both RISC and DSP processing, accompanied by an extensive collection of I/O functions and fast math (trigonometric) accelerators. The software libraries of the subsystem contain small-footprint drivers for all I/O, plus DSP functions supporting signal processing. It also includes an audio processing software library of common functions, including gain control, mixer and sample rate converter. The integrated solution is optimized for "always on" data fusion combining sensor, voice, gesture and audio processing typically implemented in IoT edge devices.

ARC Sensor and Control IP Subsystem

The DesignWare ARC Sensor & Control IP Subsystem is optimized to process data from digital and analog sensors, offloading the host processor and enabling more power-efficient processing of sensor and control data. The fully configurable IP subsystem includes the choice of an ARC EM4 or EM6 processor, serial digital interfaces, data converter interfaces and hardware accelerators. The Sensor & Control IP Subsystem provides designers with a complete and pre-verified solution that meets the requirements of a broad range of sensor processing and control functions increasingly prevalent in automotive, mobile, industrial and IoT markets.

ARC Subsystems	Supported Processors	Hardware Accelerators	Integrated Peripherals	Included Software
ARC IoT Communications IP Subsystem	EM11D	✓	SPI, UART(s), GPIO, Digital Front End (DFE), PMU and RTC	DSP library, base communications library, device drivers
ARC Data Fusion IP Subsystem	EM5D, EM7D, EM9D, EM11D	✓	SPI, I2C, I3C, PWM, UART, PDM, ADC I/F, DAC I/F, APB I/F, GPIO	DSP library, audio processing library, peripheral I/O drivers (bare metal), reference designs ARC Sensor & Control
ARC Sensor and Control IP Subsystem	EM4, EM6	✓	SPI, I2C, PWM, UART, ADC I/F, DAC I/F, APB I/F, GPIO	DSP library, peripheral I/O drivers (bare metal)

Table 1: DesignWare ARC Processor Subsystems

Software Development Support

Software Tool Chains

To accelerate the SoC development cycle, Synopsys' processor IP is supported by a complete and integrated development tool suite, including tools for configuration, software development and simulation. This enables ARC users to efficiently build, debug, profile and optimize their embedded software applications for ARC.

The ARC MetaWare Development Toolkit contains all the components needed to support the development, debugging and optimization of embedded applications for ARC processors. The compiler and debugger are fully integrated in the Eclipse-based MetaWare Integrated Development Environment (IDE), and the Toolkit also comes with a base version of the nSIM Instruction-Set Simulator.

The ARC EV Vision Processor family is supported by MetaWare EV Development Toolkit, a comprehensive, high-productivity software development environment based on common embedded vision standards, including OpenVX and OpenCL C. The tool suite enables the development of efficient computer vision applications on the EV processor's vector engine as well as automatic mapping and optimization of neural networks graphs on the dedicated DNN accelerator. The mapping tools support Caffe and Tensorflow frameworks, as well as the ONNX neural network interchange format. For maximum flexibility and future-proofing, the tool can also distribute computations between the VPU and DNN resources to support new and emerging neural networks.

In addition, Synopsys' ARC EM and HS processors are supported by the latest open-source GNU Tool Chain, including the GNU GCC Compiler, GDB Debugger, libraries and utilities.

Simulators

Synopsys offers a variety of simulation products spanning automatically-generated, cycle-accurate simulators to fast, functional instruction-set simulators (ISS). Synopsys' simulation products enable software development prior to silicon being available.

The DesignWare ARC nSIM Pro Simulator is primarily used for software development and debugging. It can operate as a very fast ISS and also supports the Synopsys Virtualizer prototyping tools. It includes a Virtualizer Development Kit (VDK) for an ARC HS38-based system. This system can boot Linux on the ARC HS38 and can be used for early software development.

DesignWare ARC xCAM is a 100% cycle-accurate simulator that is primarily used for hardware verification, but can also be used to do final optimizations of critical software routines. The xCAM model is automatically generated from the processor configuration and can be used to evaluate different hardware scenarios.

Operating Systems

To support applications that require fast, real-time response, Synopsys offers MQX RTOS. MQX occupies a very small memory footprint and supports fast context switch times.

ARC processor cores with MMUs are supported by a Linux kernel available from the official Linux archive. Synopsys maintains and optimizes the Linux kernel to run optimally on ARC processor cores.

embARC.org

The embARC.org website provides online access to a wide range of open source software and documentation for ARC processors. It provides access to downloads, documentation, mailing lists for open source projects such as ARC Linux and the embARC Open Software Platform. It also includes links to development tools and other resources for developing software on ARC processor-based systems. Users can contribute to this open source software and provide suggestions on improving or adding to the existing open source projects.

Available on embARC.org, the embARC Open Software Platform is an easily accessible, highly productive solution for developing software for ARC EM and HS processor-based embedded systems and subsystems, especially those targeting the IoT. The comprehensive suite of free and open-source software available from the embARC.org website, including drivers, operating systems and middleware, enables code development to start sooner and complete faster. Documentation and other resources available on the website facilitate the sharing of information and expertise among the ARC-based development community.

Third-party Ecosystem

The ARC Access Program expands the choice of embedded software and hardware solutions available for ARC processor cores. This program builds on the ecosystem of third parties supporting the ARC architecture with software development tools, real-time operating systems (RTOSes), middleware and semiconductor IP.

The ARC Access Program helps customers to:

- Develop ARC-based embedded solutions faster by leveraging compatible products from leading embedded industry vendors
- Reduce project risk by taking advantage of design solutions pre-ported and tested for the DesignWare ARC architecture
- Save on development costs and resources by using products optimized for ARC-based designs

ARC EM Software Development Platform

The ARC EM Software Development Platform accelerates software development and debug of ARC EM processor-based system-on-chips (SoCs) for a wide range of ultra-low power embedded applications such as IoT, sensor fusion, and voice applications. The ARC EM Software Development Platform includes a configurable hardware board with commonly used peripherals including motion sensors, flash memory, Bluetooth, and Wi-Fi and is extensible with Arduino, mikroBUS and Pmod connectors. Downloadable platform packages with hardware and software configuration information are available, providing a flexible software development platform.

Figure 1: ARC EM Software Development Platform

ARC IoT Development Kit

The DesignWare ARC IoT Development Kit accelerates software development and debug of ARC EM processor-based SoC designs. The kit includes a silicon implementation of the ARC Data Fusion IP Subsystem as well as a rich set of peripherals commonly used in IoT designs such as USB, I3C and PWM. The kit is supported by Synopsys' MetaWare Development ToolKit, which includes a compiler, debugger and libraries optimized for maximum performance with minimal code size.

Figure 2: ARC IoT Development Kit

ARC EM Starter Kit

The ARC EM Starter Kit is a low-cost, versatile solution enabling rapid software development, code porting, software debugging, and system analysis for ARC EM processors. The kit consists of a small factor board with pre-installed FPGA images supporting the range of EM cores including the EM4, EM5D, EM6 and EM7D, as well as FPU. Software support includes MQX RTOS and the embARC Open Software platform available from the embARC.org web portal.

Figure 3: ARC EM Starter Kit

ARC HS Development Kits

The ARC HS Development Kits are ready-to-use software development platforms that include a multicore ARC HS3x-based or ARC HS4xD-based chip, implemented in a TSMC 28HPM process, that integrates a wide range of interfaces including Ethernet, USB, SDIO, I2C, SPI, UART, and GPIO, as well as a GPU. The kit also features an on-board WiFi and Bluetooth module. This combination of ARC HS processors and the comprehensive set of peripherals allow developers to build and debug complex software on a fully-featured hardware platform. Software support includes ARC Linux and the embARC Open Software platform available from the embARC.org web portal.

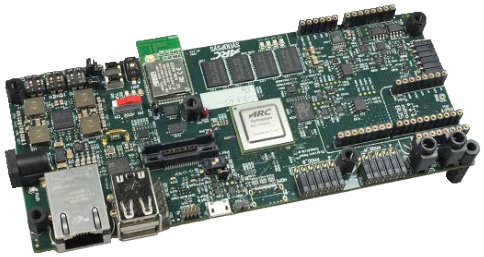


Figure 4: ARC HS Development Kit

ARC AXS10x Software Development Platforms

The DesignWare ARC Software Development Platforms are complete, standalone platforms enabling software development, code porting, software debugging and system analysis. They consist of an ARC CPU card mounted on an ARC Software Development Platform mainboard. The CPU cards have an associated software package of pre-built operating systems, drivers and examples. Readily licensable DesignWare IP has been used to build the ARC Software Development Platforms, giving the systems a rich set of peripherals that can also be implemented in an SoC. The ARC Software Development Platforms can easily be combined with the Synopsys HAPS® FPGA-Based Prototyping Solution to enable system prototyping and additional extension interfaces, such as five Digilent Pmod™ Compatible connectors, support the integration of other custom and commercially available hardware extensions.

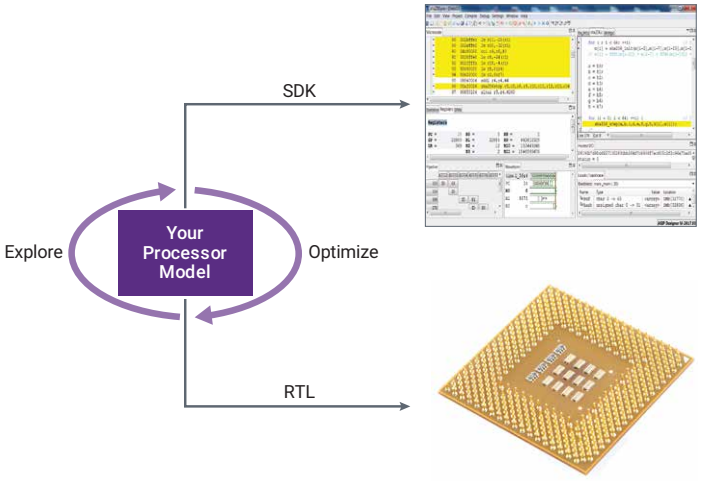
Figure 5: ARC AXS103 Software Development Platform

ASIP Designer

Modern multicore SoCs often include specialized processing functions that sometimes cannot be addressed efficiently with off-the-shelf processor IP. These custom processing elements are often manually designed, requiring significant engineering effort and lacking ease-of-use features such as programmability. Application-specific instruction-set processors (ASIPs) close this gap.

ASIPs are software-programmable hardware (e.g., custom processors or programmable accelerators) tailored to a specific application or class of algorithms. They are ideally suited for specialized DSP applications, enabling designers to take advantage of inherent instruction- and data-level parallelism and customized datapath elements to achieve high levels of performance in a minimal power envelope. Because they are programmable, ASIPs also give design teams the flexibility to support post-silicon modifications as well as specifications that are still evolving.

ASIP Designer is a tool suite to accelerate the design and verification of ASIPs that brings ASIP design within easy reach of every SoC team. Using a single processor description language, ASIP Designer automatically generates both a software development kit (SDK) including a C/C++ compiler, both cycle-accurate and instruction-accurate simulators, and a fully featured debugger, as well as synthesizable RTL. This allows for efficient exploration of architectural choices and a rapid path to silicon implementation.



DesignWare Processor Families

ARC EM Family—Ultra-Compact, Ultra Low-Power Processors for Deeply Embedded Applications							
Key Features	**EM4**	**EM6**	**EM5D**	**EM7D**	**EM9D**	**EM11D**	**EM22FS**
3-stage pipeline based on ARCv2 ISA	✓	✓	✓	✓	✓	✓	✓
Up to 2 MB instruction and data closely coupled memory	✓	✓	✓	✓	✓	✓	✓
Enhanced sleep modes	✓	✓	✓	✓	✓	✓	✓
Arm® AMBA® AHB and AHB-Lite™ interfaces	✓	✓	✓	✓	✓	✓	✓
32 KB of instruction and data caches		✓		✓		✓	✓
DSP enhanced ARCv2DSP ISA with 150+ DSP instructions and 32x32 MUL/MAC			✓	✓	✓	✓	✓
Up to 8 registers for fast context switch	✓	✓	✓	✓	✓	✓	✓
Programmable watchdog timer	✓	✓	✓	✓	✓	✓	✓
32x32 MUL/MAC unit			✓	✓	✓	✓	✓
XY memory					✓	✓	
Power management interface/DVFS support	✓	✓	✓	✓	✓	✓	✓
ECC on memories	✓	✓	✓	✓	✓	✓	✓
Enhanced Security Package	Opt		Opt				Opt
µDMA controller	Opt	Opt	Opt	Opt	Opt	Opt	Opt
CryptoPack (cryptographic software algorithm acceleration)	Opt	Opt	Opt	Opt	Opt	Opt	Opt
FPU (single- and double-precision, IEEE754-2008 compliant)	Opt	Opt	Opt	Opt	Opt	Opt	Opt
Memory Protection Unit (MPU)	Opt	Opt	Opt	Opt	Opt	Opt	✓
Real-Time Trace (RTT)	Opt	Opt	Opt	Opt	Opt	Opt	Opt
ARConnect (ARC EM multicore connect IP)	Opt	Opt	Opt	Opt			
Example Applications							
IoT, wearables, sensor processing and control, smart appliances, always-on sensors, SSDs, flash controllers, automotive safety systems (ISO 26262)							

Opt = separately licensable options

ARC SEM Family—Security Processors for Low-Power Embedded Applications			
Key Features	**SEM110**	**SEM120D**	**SEM130FS**
3-stage pipeline based on ARCv2 ISA	✓	✓	✓
Up to 2 MB instruction and data closely coupled memory	✓	✓	✓
Secure privilege mode orthogonal to kernel/user mode	✓	✓	✓
Enhanced secure MPU with context ID for secure or normal operation	✓	✓	✓
Up to 16 configurable protected regions and per region scrambling capability	✓	✓	✓
Uniform instruction timing	✓	✓	✓
Timing/power randomization	✓	✓	✓
In-line instruction scrambling	✓	✓	✓
Data and instruction path integrity checking	✓	✓	✓
Integrated watchdog timer	✓	✓	✓
Secure debug capability with user-defined challenge/response mechanism	✓	✓	✓
DSP-enhanced ARCv2DSP ISA with 100+ DSP instructions and 32x32 MUL/MAC		✓	✓
Functional Safety			✓
µDMA controller	Opt	Opt	Opt
CryptoPack (cryptographic software algorithm acceleration)	Opt	Opt	Opt
FPU (single- and double-precision, IEEE754-2008 compliant)	Opt	Opt	Opt
Example Applications			
IoT industrial, smart cities, smart meters, embedded SIM, healthcare, automotive			

Opt = separately licensable options

DesignWare Processor Families (Continued)

HS3x and HS4x/D Processors (ARCv2 ISA)—High-Speed 32-bit Processors for High-End Embedded Applications											
Key Features	**HS34**	**HS36**	**HS38**	**HS44**	**HS46**	**HS48**	**HS45D**	**HS47D**	**HS46FS**	**HS47DFS**	**HS48FS**
10-stage pipeline based on ARCv2 ISA	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Dual-issue pipeline				✓	✓	✓	✓	✓	✓	✓	✓
Up to 16 MB instruction and data closely coupled memory (CCM)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
64-bit loads and stores	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Up to 8 register files for fast context switching	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Arm® AMBA® AXI™ and AHB-Lite™ interfaces	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Single-, dual- and quad-core configurations	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
64 KB of instruction and data caches		✓	✓		✓	✓		✓	✓	✓	✓
Enhanced sleep modes and architectural clock gating	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
DSP enhanced ARCv2DSP with 150+ DSP instructions							✓	✓		✓	
L1 and I/O cache coherency		✓	✓		✓	✓		✓	✓	✓	✓
64-bit ARC Processor EXtensions (APEX)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
ECC on memories	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
32x32 MUL/MAC unit	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Power management interface/DVFS support	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Memory Management Unit (MMU) supporting 40-bit addressing		Opt	✓		Opt	✓		Opt	Opt	Opt	✓
L2 cache		Opt	✓		Opt	✓		Opt	Opt	Opt	✓
Enhanced Security Package	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt
FPU (single- and double-precision, IEEE754-2008 compliant)	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt
Memory Protection Unit (MPU)	Opt	Opt		Opt	Opt		Opt	Opt	Opt	Opt	Opt
Cluster DMA	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt
Real-Time Trace (RTT)	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt	Opt
Example Applications											
Solid state drive (SSD) controller, automotive systems, home gateways, baseband control, home networking, edge devices, embedded Linux-based devices											

Opt = separately licensable options

DesignWare Processor Families (Continued)

ARC HS5x and HS6x Processors (ARCv3 ISA)—High-Speed 32-/64-bit Processors for High-End Embedded Applications					
Key Features	**HS56**	**HS57D**	**HS58**	**HS66**	**HS68**
10-stage pipeline based on ARCv2 ISA	✓	✓	✓	✓	✓
Dual-issue pipeline	✓	✓	✓	✓	✓
Up to 16 MB instruction and data closely coupled memory (CCM)	✓	✓	✓	✓	✓
64-bit loads and stores	✓	✓	✓		
128-bit loads and stores				✓	✓
Up to 8 register files for fast context switching	✓	✓	✓	✓	✓
Arm® AMBA® AXI™ and AHB-Lite™ interfaces	✓	✓	✓	✓	✓
Up to 12-core configurations	✓	✓	✓	✓	✓
64 KB of instruction and data caches	✓	✓	✓	✓	✓
Enhanced sleep modes and architectural clock gating	✓	✓	✓	✓	✓
DSP enhanced ARCv2DSP with 150+ DSP instructions		✓			
L1 and I/O cache coherency	✓	✓	✓	✓	✓
64-bit ARC Processor EXtensions (APEX)	✓	✓	✓		
128-bit ARC Processor EXtensions (APEX)				✓	✓
ECC on memories	✓	✓	✓	✓	✓
32x32 MUL/MAC unit	✓	✓	✓		
2x 32x32 MUL/MAC unit				✓	✓
Power management interface/DVFS support	✓	✓	✓	✓	✓
Memory Management Unit (MMU) supporting 40-bit addressing			Opt		Opt
52-bit physical, 64-bit virtual address space				Opt	Opt
L2 cache	Opt	Opt	Opt	Opt	Opt
Enhanced Security Package	Opt	Opt	Opt	Opt	Opt
FPU (single- and double-precision, IEEE754-2008 compliant)	Opt	Opt	Opt		
128-bit SIMD FPU IEEE754 compliant				Opt	Opt
Memory Protection Unit (MPU)	Opt	Opt	Opt	Opt	Opt
Cluster DMA	Opt	Opt	Opt	Opt	Opt
Real-Time Trace (RTT)	Opt	Opt	Opt	Opt	Opt
Example Applications					
Solid state drive control, automotive systems, wireless modems, networking, IoT nodes and gateways					

Opt = separately licensable options

DesignWare Processor Families (Continued)

ARC VPX Family—High-Performance DSP for Signal Processing Applications						
Key Features	**VPX2**	**VPX3**	**VPX5**	**VPX2FS**	**VPX3FS**	**VPX5FS**
Vector-length (bit)	128	256	512	128	256	512
ARCv2 ISA support	✓	✓	✓	✓	✓	✓
Scalar execution unit	✓	✓	✓	✓	✓	✓
Three vector execution units	✓	✓	✓	✓	✓	✓
Dual SIMD multiply units (8-, 16- and 32-bit)	✓	✓	✓	✓	✓	✓
Dual floating point vector engines (half and single precision)	✓	✓	✓	✓	✓	✓
Linear algebra/math vector floating point engine	✓	✓	✓	✓	✓	✓
Vector data closely coupled memory (VCCM)	✓	✓	✓	✓	✓	✓
Arm® AMBA® AXI™ and AHB-Lite™ interfaces	✓	✓	✓	✓	✓	✓
Single-, and dual-core configurations	✓	✓	✓	✓	✓	✓
Quad-core configurations			✓			✓
Enhanced sleep modes and architectural clock gating	✓	✓	✓	✓	✓	✓
L1 and I/O cache coherency unit	✓	✓	✓	✓	✓	✓
ECC on memories	✓	✓	✓	✓	✓	✓
Safety certified				✓	✓	✓
Power management interface/DVFS support	✓	✓	✓	✓	✓	✓
L2 cache	Opt	Opt	Opt	Opt	Opt	Opt
Scalar FPU (single- and double-precision, IEEE754-2008 compliant)	Opt	Opt	Opt	Opt	Opt	Opt
Memory Protection Unit (MPU)	Opt	Opt	Opt	Opt	Opt	Opt
2D DMA engine	Opt	Opt	Opt	Opt	Opt	Opt
Real-Time Trace (RTT)	Opt	Opt	Opt	Opt	Opt	Opt
Example Applications						
Automotive driver assist systems (ADAS), RADAR, LiDAR, powertrain, engine control, multi-sensor fusion, baseband comunications, industrial automation, smart home, IoT, and voice/speech/natural language processing						

Opt = separately licensable options

EV Family—Fast, Accurate Object Detection for Embedded Vision Applications						
Key Features	**EV71**	**EV72**	**EV74**	**EV71FS**	**EV72FS**	**EV74FS**
# vector processing units	1	2	4	1	2	4
Vector engine MACs	64	128	256	64	128	256
DMA option	✓	✓	✓	✓	✓	✓
L1 cache coherency		✓	✓		✓	✓
DNN/CNN Engine option (MACs)	880, 1760, or 3520	880, 1760, or 3520	880, 1760, or 3520	880, 1760, or 3520	880, 1760, or 3520	880, 1760, or 3520
Vector floating point unit option	✓	✓	✓	✓	✓	✓
Real-time trace (RTT)	✓	✓	✓	✓	✓	✓
Functional safety				Integrated (ASIL B, C, or D)	Integrated (ASIL B, C, or D)	Integrated (ASIL B, C, or D)
Example applications						
Autonomous vehicles, ADAS, surveillance, facial detection/recognition, augmented reality, SLAM						

DesignWare Processor Families (Continued)

ARC AS200 Audio Family—Efficient Single/Dual Core Audio Processors, Optimized Codecs		
Key Features	**AS211SFX**	**AS221BD**
5-stage pipeline	✓	✓
Dual MAC with 80-bit accumulator	✓	✓
AMBA AXI or BVCI interfaces	✓	✓
ARC-optimized audio codecs support Dolby, DTS, Microsoft, SRS technologies and more	✓	✓
Dual-core configuration		✓
Floating point extensions (single and double-precision, IEEE compliant)	Opt	Opt
Memory Protection Unit (MPU)	Opt	Opt
Real-Time Trace (RTT)	Opt	Opt
Example Applications		
Portable audio players, digital TVs, set-top boxes, sound bars, multi-channel HD, wireless headsets and speakers		

Opt = separately licensable options

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, PVT sensors, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors, and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits, and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enable designers to reduce integration risk and accelerate time-to-market.

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