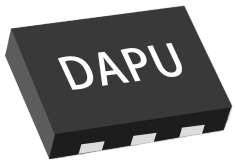
10kHz to 350MHz Silicon Oscillator Series

DSO3001

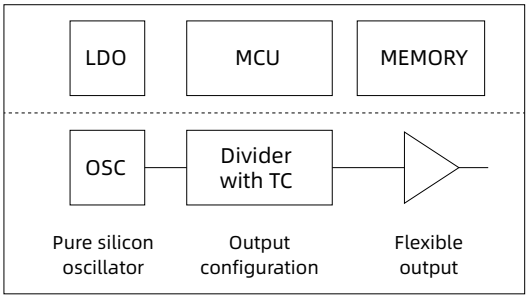


The DSO3001 All-Silicon Oscillator adopts advanced frequency synthesis and sensor (temperature sensor and stress sensor) technology, and provide a low-jitter clock at high frequencies. The device is programmable and can generate clock signals at any frequency and multi-format signal in the range of 10kHz to 350MHz. Built-in LDO and power filter greatly improve the chip's power noise suppression ability, and DSO3001 supports switching power supply. DSO3001 is all-silicon oscillator, so it has high reliability and could work in harsh environment (including strong vibration).

Features:

- Quartz free and MEMS parts
- Single-end output: 10kHz ~ 212.5MHz
- Differential output: 10kHz ~ 350MHz
- LVDS, LVPECL, HCSL, CML, LVCMOS or dual LVCMOS output
- Jitter as low as 350 fs RMS@12 kHz ~ 20 MHz
- Compliance with PCIe Gen1/2/3/4/5
- Frequency stability: ±50ppm
- Built-in LDO and power filter circuit
- Power supply range: 1.8V ~ 3.3V
- Operation temperature range: -40℃ ~ +85℃

Block Diagram

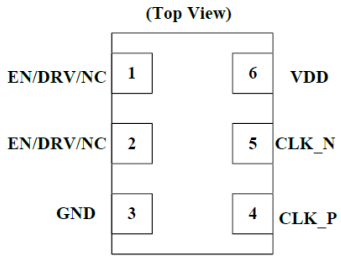


Application

- Optical modules
- SONET/SDH
- FPGA/ASIC clock generation
- Networking switches and gateways
- System clocking
- Storage, servers and datacenters
- 100G/200G/400G/800G ethernet switches and routers

Pin Function

PIN	Description
1,2	Optional function EN=Output enable, high level active DRV=Output driver enable, high level active NC = Not connect
3	GND= Ground
4	CLK_P = Clock output
5	CLK_N = Complementary clock output
6	VDD = Power supply



5.0x3.2mm and 3.2x2.5mm

Selected Electrical Specifications VDD=2.5V or 3.3V ±10%, Ta= -40 ~ +85°C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Frequency range	F_{CLK}	LVDS, LVPECL, CML, HCSL	0.01	-	350	MHz
		CMOS, Dual CMOS	0.01	-	212.5	
Supply voltage	V_{DD}	-	1.71	1.8	1.89	V
			2.375	2.5	2.625	
			3.135	3.3	3.47	
Supply Current	I_{DD}	-	-	-	80	mA
Operating temp.	Ta	-	-40	+25	+85	°C
Total stability	Δf/f	Ta= -40°C ~ + 85°C	-50	-	+50	x 10^{-6}
Rise/fall time (20% to 80% VPP)	T_R/T_F	LVPECL/LVDS/CML	-	-		ps
		CMOS / Dual CMOS (CL = 5 pF)	-	0.5	1.5	ns
		HCSL, FCLK >50 MHz	-	-	550	ps
Start up time	t_{OSC}	Time from 0.9 × VDD until output frequency (FCLK) within spec	-	-	4	ms
Phase jitter (RMS) for F_{CLK} ≥ 10 MHz	ΦJ	12 kHz to 20 MHz integration BW2	-	350	750	fs
Phase jitter (RMS) for F_{CLK} ≥ 156.25 MHz	ΦJ		-	155	250	ps
Duty cycle	DC	All formats	45	-	55	%
Output enable (OE/DRV)	V_{IH}		0.7xV_{DD}	-	-	V
	V_{IL}		-	-	0.3xV_{DD}	V
LVPECL output option	V_{OC}	Mid-level	V_{DD}-1.55	-	V_{DD}-1.25	V
	V_O	Swing (diff)	1.4	-	1.85	V_{pp}
LVDS output option	V_{OC}	Mid-level (2.5V/3.3V V_{DD})	1.125	1.20	1.275	V
		Mid-level (1.8V V_{DD})	0.795	0.85	0.906	V
	V_O	Swing (diff)	0.5	0.82	0.96	V_{pp}
	V_{OI}		-	5	10	mV
HCSL output option	V_{OH}	Output voltage high	695	820	945	mV
	V_{OI}	Output voltage low	-	5	10	mV
CML output option	V_O	Swing (diff)	0.725	0.8	0.89	V_{pp}
CMOS output option	V_{OH}		0.83xV_{DD}	-	-	V
	V_{OI}		-	-	0.17xV_{DD}	V