ACCELERCOMM
SUPERCHARGED WIRELESS

5G NR LDPC Product Overview

July 2020

Key features and benefits of our LDPC product suite for 5G New Radio Applications.

INTRODUCTION

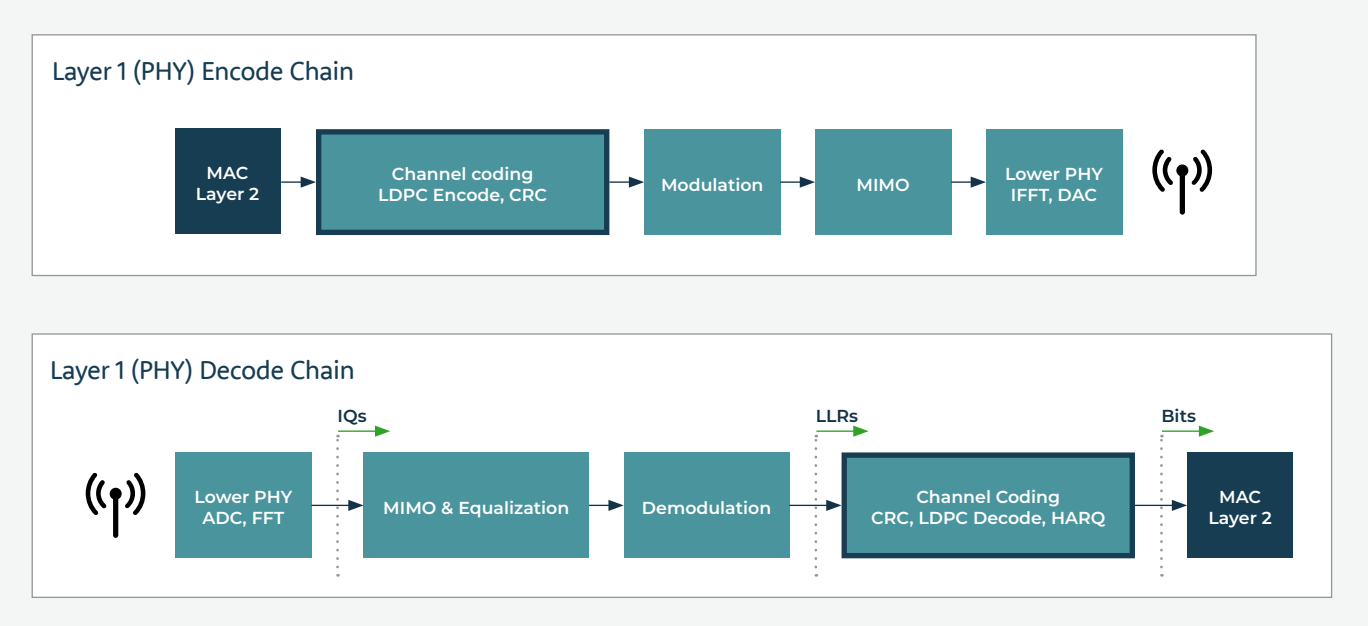
AccelerComm's 5G NR LDPC solutions are optimised for the specific needs of the 3GPP 5G New Radio (NR) standards to provide market leading performance and efficiency. The product suite includes a complete encoder and decoder solution that delivers reduced latency and power consumption for one of the most critical components of the physical layer, whilst performing to all the 3GPP specified throughput and error correction targets. The Flexible IP packages can be quickly integrated into FPGA, ASIC or software designs.

INTRODUCTION

3GPP 5G New Radio (NR) is designed to work across a wide range of use cases delivering unprecedented performance and flexibility from 20Gbps broadband to sub millisecond ultra low latency applications. These requirements present a unique set of challenges for channel coding.

Channel coding or Forward Error Correction (FEC) refers to the process where extra protection bits are added to the information bits before transmission. At the receiver a decoder uses complex algorithms to extract the original information bits from the received data, correcting for errors introduced by interference and fading.

5G NR introduces the use of a Low Density Parity Check (LDPC) channel coder for the Physical Uplink and Downlink Shared Channels (PUSCH and PDSCH) over which user data is passed. LDPC is already in use in WiFi and satellite broadcast applications but the variant used in 5G NR is significantly more flexible to support the full range of performance required. It has thousands of possible configurations, as opposed to the handful used in other standards. With the LDPC decoder consuming up to 40% of the resources needed to realise the 5G NR Physical Layer (PHY), decoder performance and efficiency are fundamental to the performance of the overall receiver.



BENEFITS

The AccelerComm™ LDPC decoder product suite has been specifically designed as flexible IP to address the unique challenges of 5G NR across all use cases covered by the current standards, deliver market leading performance and efficiency, and be easily integrated into designs.

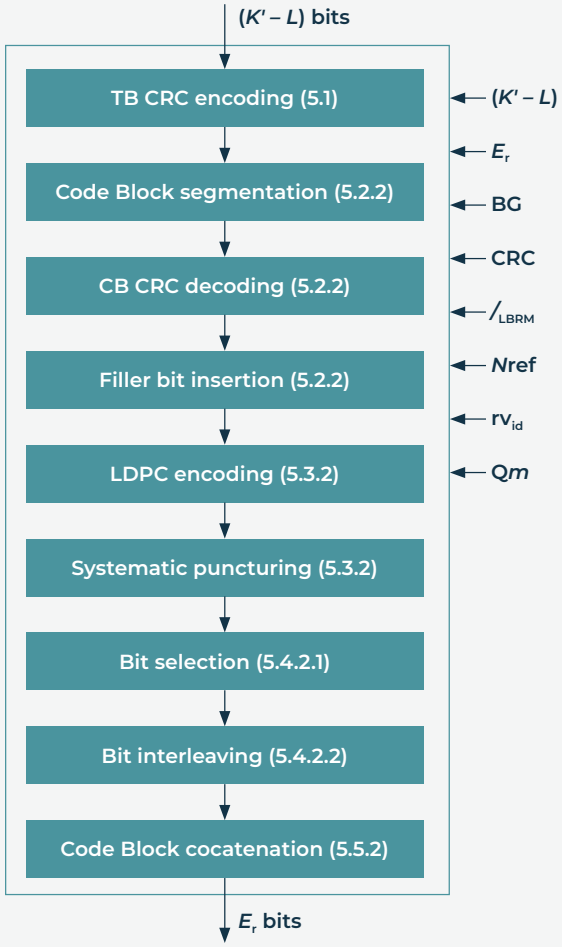
Key features include:

- Complete implementation of the LDPC part of TS 38.212
- Supported across FPGA, ASIC and Software platforms
- Highly configurable for a wide range of base station (gNB) and terminal (UE) applications
- 5G NR optimised design outperforms generic solutions
- Configurable to support maximum throughputs and minimum timing requirements for all numerologies
- Very low latency – meets strictest requirements for URLLC
- Efficient design – saves device area
- Low power – half the energy per bit of competitors
- Easy to integrate
- No error floors

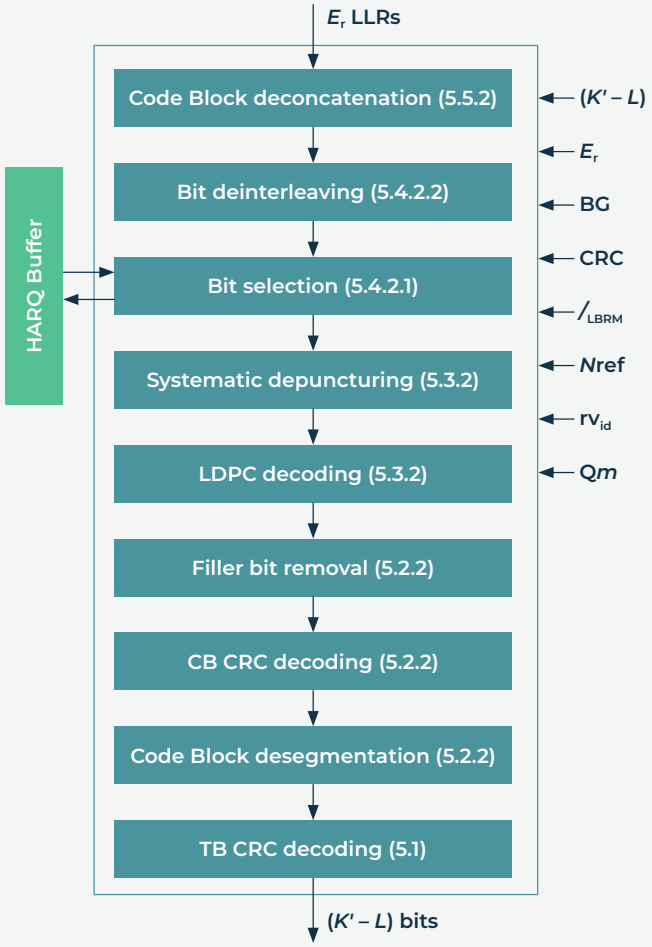
FUNCTIONALITY

As well as the core encoding and decoding functionality the AccelerComm™ solution includes all the other LDPC functionality required by the 3GPP TS 38.212 channel coding standard. Of particular note is support for Hybrid Automatic Repeat Request (HARQ). A block of data, referred to as a Transport Block (TB), is sent over the air interface composed of many Code Blocks (CBs). After decoding, each CB is checked for correctness with a Cyclic Redundancy Check (CRC). If any CBs fail, the receiver system requests the retransmission of just those CBs not the entire TB. When retransmission is received, the decoder combines it with the original and retries the decode. If this is successful it inserts the decoded bits into the transport block. Functionality to support this process and interface to a HARQ buffer provided by external DRAM is included.

The IP is fully configurable, and key additional functions can be disabled if not required. By providing the complete 3GPP specified functionality in a single IP package, development time is dramatically reduced.



LDPC encoder chain functionality
(numbers in brackets correspond to sections of 3GPP TS 38.212)



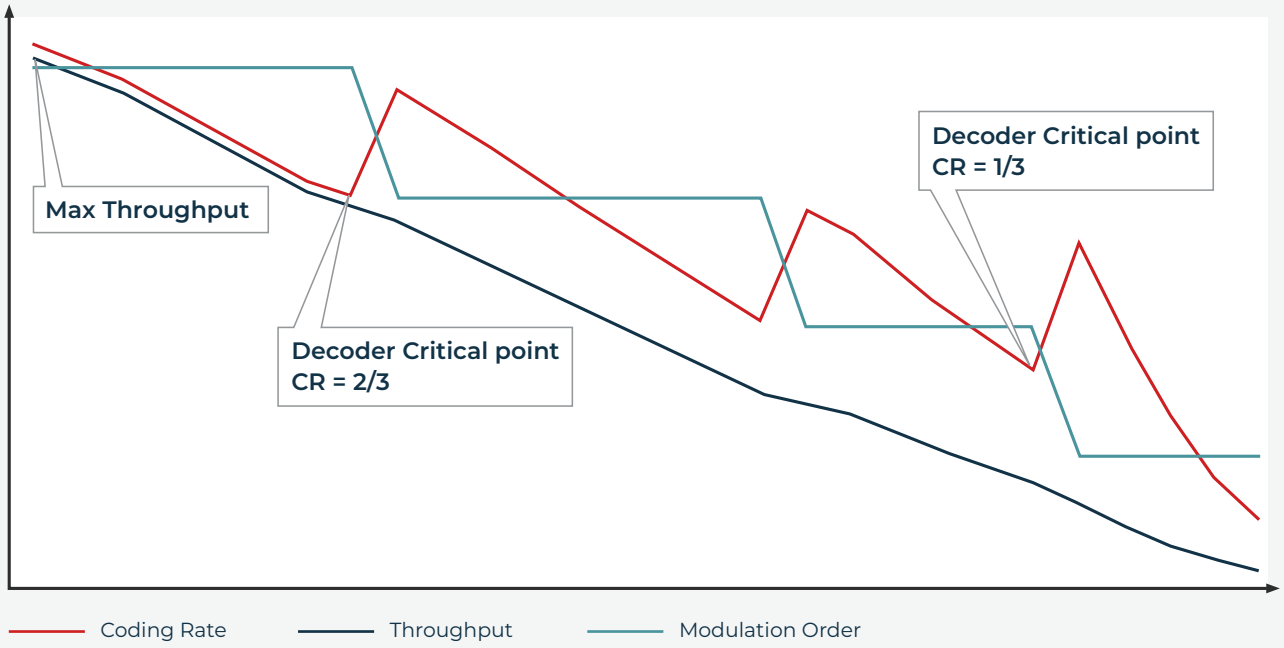
LDPC decoder chain functionality
(numbers in brackets correspond to sections of 3GPP TS 38.212)

THROUGHPUT PERFORMANCE

5G NR supports throughputs of up to 20Gbps, in favourable radio environments and then adapts when conditions such as interference and fading vary by changing the Modulation Coding Scheme (MCS). Changing the MCS has the effect of increasing or decreasing the ratio of protection bits to information, referred to as the coding rate. When the radio link is likely to introduce more errors, more protection bits are used and significantly more processing is required at the decoder.

The decoder must be able to achieve the required throughput at all coding rates and often this is achieved by specifying the decoder based on the most challenging coding rate. For some decoder architectures this means they are over specified, wasting resources. The unique architecture of the AccelerComm™ decoder closely matches the required profile to deliver the required performance with significantly reduced area and power usage.

5G NR Modulation Coding Scheme (MCS) Index table 2 (256QAM)



LATENCY

Reducing the time taken between a block of data being sent from the transmitter to being received by the user, known as latency, is a major focus of 5G. Use cases from mobile gaming to industrial automation have driven 5G to set a target of a 10X reduction from the latency provided by 4G, whilst still maintaining a reliable link. 4G requirements meant the channel coders had to operate within a processing time window of the order of 1 millisecond. Studies have shown that the 5G requirements will need decoders to be capable of working in a processing time window below 10 microseconds.

The unique AccelerComm™ architecture is designed to deliver low processing times from the outset and can meet the strictest requirements of 5G without a significant increase in the resources required.

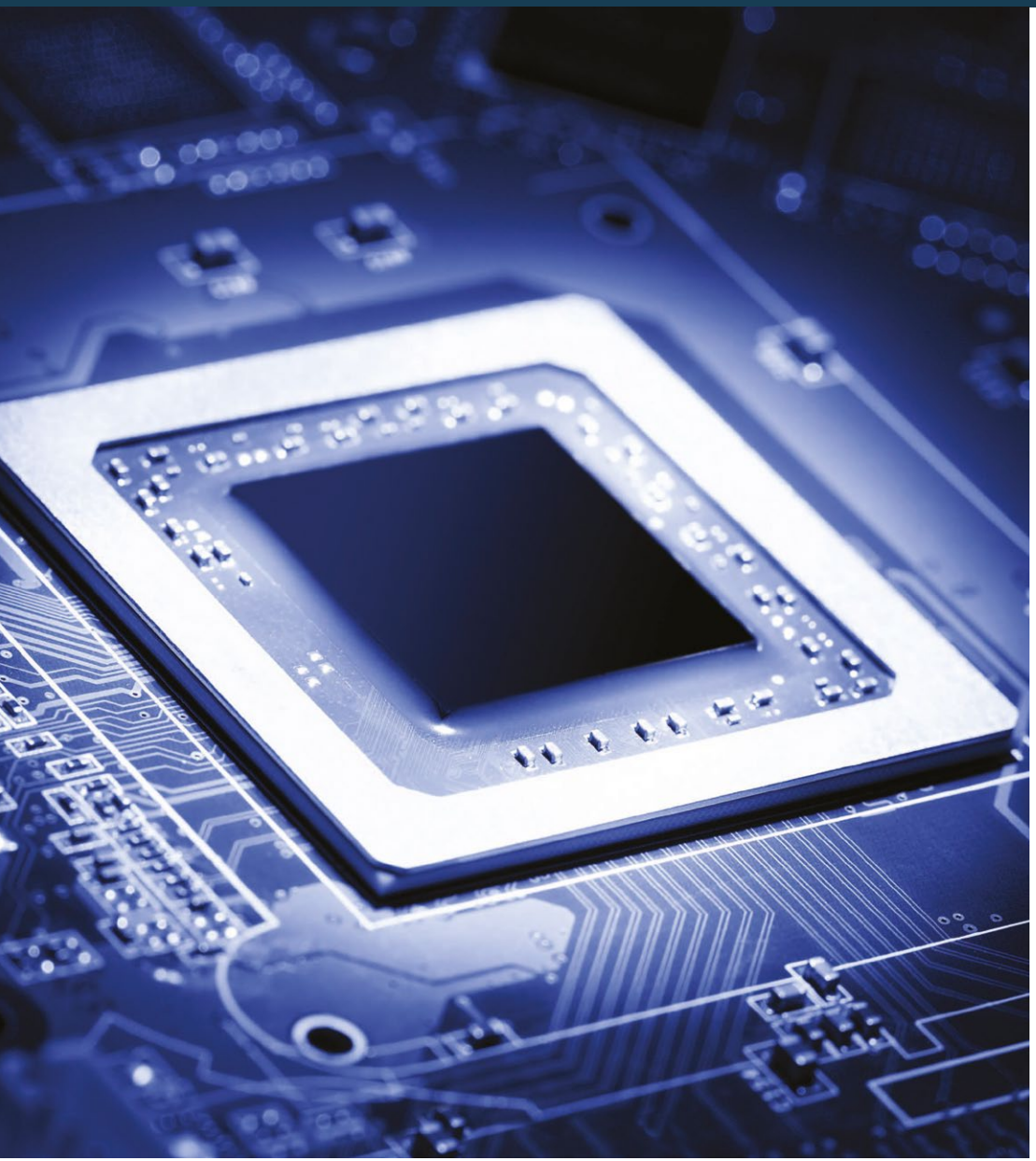
ERROR CORRECTION PERFORMANCE

The decoder must achieve a low Block Error Rate (BLER) across a wide range of input signal conditions or Signal to Noise Ratios (SNRs), and at all coding rates. The AccelerComm™ decoder achieves performance up to 0.4dB better than general purpose decoders. And within 0.1dB of the theoretical maximum. Improved error correction performance leads to fewer HARQ retries, reduced latency and increased system capacity and efficiency.

A known challenge of all LDPC decoders is a phenomenon called 'error floors' where performance improvement with good SNR tails off at very low error rates. The AccelerComm™ decoder can be configured to completely eliminate these, which will be critical for envisaged ultra reliable 5G use cases.

Typical LDPC decoder latency requirements

SCS (KHz)	Slot length (µs)	Symbol time (µs)	Maximum L1/2 delay (Symbols)	Maximum L1/2 delay (µs)	Maximum LDPC decode processing delay (µs)
30	500.0	35.7	2.0	71.4	**23.8**
60	250.0	17.9	3.0	53.6	**17.9**
120	125.0	8.9	4.0	35.7	**11.9**



HARDWARE RESOURCE USAGE

By using a design optimised for the characteristics of the 5G NR LDPC standard the AccelerComm™ IP uses typically 20% to 40% less resources (chip area) in an FPGA or ASIC than the best general-purpose decoders designed for the same throughput, whilst delivering lower latency and consuming less power.

For example a gNB decoder capable of supporting the maximum throughput at all coding rates for frequencies below 6GHz, maximum use of MIMO and maximum bandwidth consumes just 14% of a Xilinx Virtex UltraScale+ VU9P FPGA per cell.

HARDWARE POWER USAGE

As well as the power consumption reductions from reduced area the AccelerComm™ design makes efficient use of memory. Memory reads and writes consume power and so reducing unnecessary memory access reduces power usage even further compared to many traditional designs.

Put together these design features result in energy usage per bit typically half that of industry leading general-purpose decoders for the same throughput requirement. For example the gNB FPGA example above consumes below 0.9nJ/bit.

SOFTWARE PERFORMANCE

The software solution is integrated into the Intel's FlexRAN Reference Software and delivers throughput up to three times that of alternate implementations. The LDPC decoder makes use of use of the powerful Intel Advanced Vector Extension 512 (Intel AVX512) instruction sets, to meet throughput and error correction requirements on Intel Xeon scalable processors and with fewer cores.

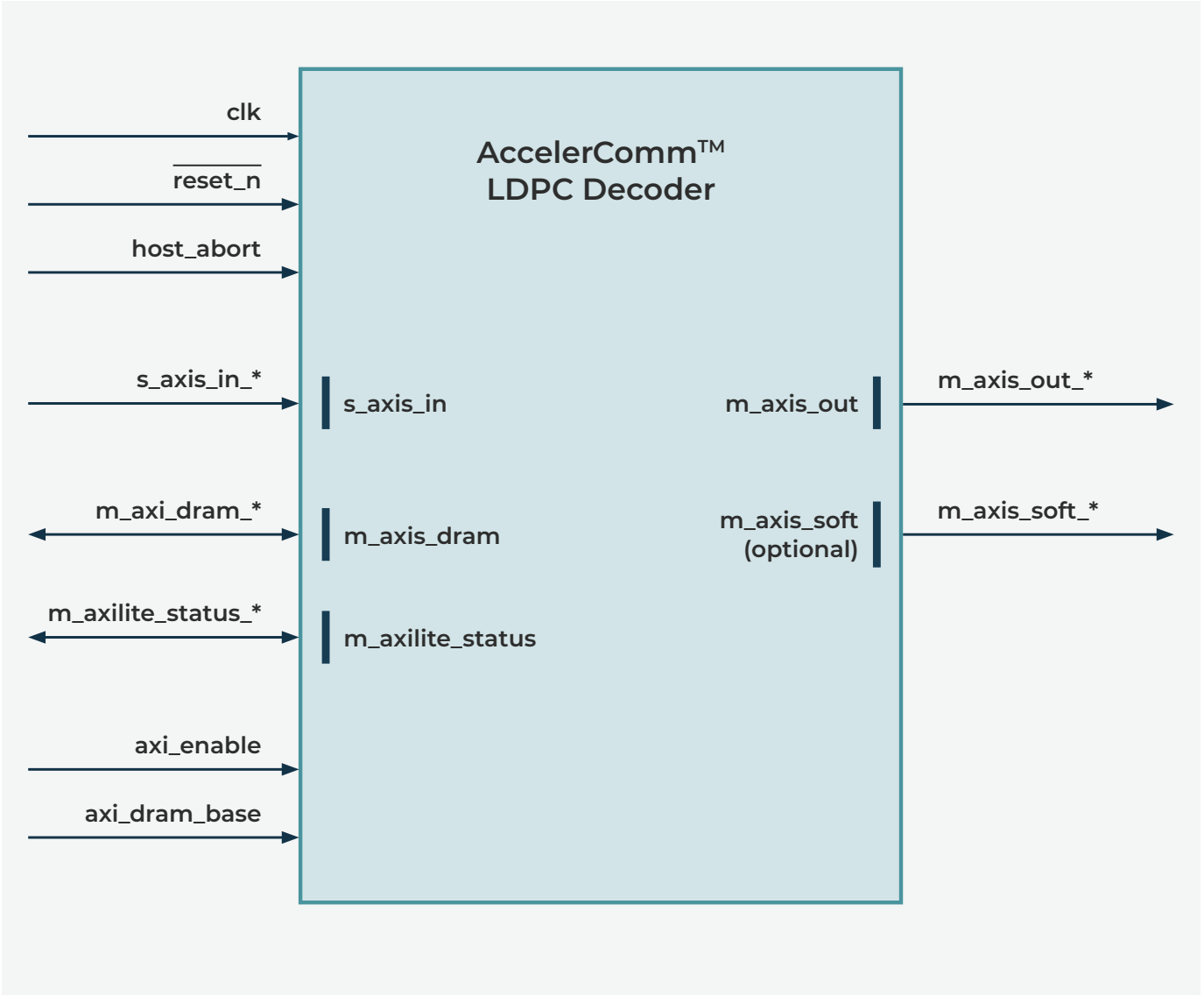
EASE OF INTEGRATION

The AccelerComm™ encoder, decoder and supporting functions are delivered as a package ready to integrate into the complete ASIC, FPGA or software design. For FPGA and ASIC the products are delivered as a netlist or RTL code which can be quickly integrated into the industry standard development environments for Intel, Xilinx and Achronix devices.

Once loaded into the development environment the functional blocks can be integrated into the users design just like any other vendor or 3rd party library. The blocks use industry standard AXI4 interfaces, one for input, one for output and an AXI4 DRAM and memory controller interface for the memory used for HARQ storage. A single clock domain is used across the IP delivered.

Key parameters such as input, core and output parallelism and interface data width are fully design time configurable to match the requirements of the rest of the design.

Error trapping and reporting is supported to quickly identify a wide range of problems and further reduce design cycles.



DESIGN SUPPORT

As well as detailed documentation the package includes a full test bench to prove 3GPP conformance that can be used in the most popular simulation tools, Mentor ModelSim® or Questa® and Cadence Xcelium®, and a bit accurate C model is also included for use in user simulations or in MATLAB.

The test bench code is provided as clear text source and so can be used by designers as an example and template for how to drive the encoder and decoder in the final design.

AccelerComm™ provides support services to customers to help them with the integration of the IP into their designs, but typically this is a very straightforward process.

Our flexible IP can be configured to closely match the requirements of a wide range of designs, and then the combination of simple interfaces, complete documentation and supporting test harnesses and reference kits, backed up by our experienced support team mean that IP can be integrated and running within a day.

REFERENCE KIT

AccelerComm™ also provides support for the BBDEV API and a complete reference kit with the LDPC decoder running on an FPGA development board over a PCIe bus is available. This reference kit shortens design time and enables the IP to be rapidly integrated and evaluated.

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AccelerComm™ is a semiconductor IP-core company that provides patented channel coding solutions. Our team has a proven track-record of channel coding and IP expertise, from developing and optimising algorithms through to their implementation and delivery in FPGA and ASIC architectures. With more than 100 published IEEE papers and numerous citations for our work in 3GPP RAN1, we are having a significant impact on the mobile communications world.

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