OCT 3032

Next Generation System-on-Chip

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The OCT3032

System-on-Chip (SoC) is a very low-power, high-performance, multi-core digital signal processor (DSP), coupled with an on-chip quad-core Arm® Cortex®-A7 processor, a set of advanced hardware accelerators, and a complete software development suite.

OCT3032 features

High-performance multi-core SoC
- Up to 32 Opus3 DSP cores
- Full support for C and C++ programming
- Software compatible with Opus2
- Advanced IDE support

Hardware acceleration
- Wireless accelerators
  - LTE Turbo encoding at 1 Gbps DL rate
  - LTE Turbo decoding at 1 Gbps UL rate
  - Simultaneous 2G/3G Turbo & Viterbi
  - Chip rate acceleration (RACH, Path Search)
- Security protocol accelerator
  - Supports AES (FIPS Pub 197, all key sizes, multiple cipher modes), SHA-384 (FIPS Pub 180-4), SNOW 3G, ZUC, and KASUMI algorithms, as well as TRNG
- Video accelerators
  - H.265/H.264 encoder/decoder
  - Image processing
- Other accelerators
  - LDPC ARJA encoder/decoder
  - LDPC DVB-S2X encoder/decoder

High speed external interfaces
- PCIe Gen2 (5 Gbps per lane), x1,x2
- Four Gigabit Ethernet MACs with parallel and SGMII modes
- Four USB 2.0 ports

Embedded application processor
- 800MHz quad-core Arm Cortex-A7
- Secure custom booting capability
- Arm CoreSight™ support

RF interfaces
- One JESD204B serial interface with up to four lanes, 6.144 Gbps per lane
- One JESD207 controller with up to three 16-bit antenna interfaces

Memory/storage interfaces
- 32-bit LPDDR4 interface
- One SD/SDIO interface
- One eMMC interface

Video/audio interfaces
- Two CSI-2 interfaces for camera input
- One LCD MIPI DSI display interface
- Two I²S audio interfaces

TDM interface
- 16 data streams
- Data rates from 2.048 Mbps to 32.768 Mbps
- Up to 2048 timeslots (DS0s)

Low speed control interfaces
- Two I²C interfaces
- Four serial peripheral interfaces, independently configurable for SPI, SSP, or Microwire
- Two UART interfaces
- 32 General Purpose I/O (GPIO) pins

OCT3032 benefits

- Flexible device architecture supports a diverse range of applications with scalable capacities
- Highest efficiency fixed-point SoC in the industry and extensive power management make it ideal for compact handheld products
- Feature-rich software development environment facilitates custom applications and features
- Proven software for 2G, 3G, 4G, and 5G accelerates wireless base station and UE product development
- Complete solution for high-density media processing offers carrier-grade features including wideband codec transcoding, conferencing, echo cancellation, and more

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OCT3032 target applications

Base station applications
- Small cells: Femtocell, Picocell, Microcell
- All variants of 2G, 3G, 4G, and 5G air interfaces
- Up to four simultaneous air interfaces of any standard
- Specialty base stations requiring custom software

UE applications
- 4G and 5G UE applications with video processing
- UE applications requiring low power and custom software

Audio transcoding applications
- Session Border Controllers, Media Gateways and PBX
- Acceleration for cloud processing and virtualized environments
- EVS and AMR-WB transcoding for VoLTE and Vo5G networks

OCT3032 performance

LTE throughput
- 2 carriers of MIMO 4x4 DL, 2x2 UL, 20 MHz
- 300 Mbps peak data rate (full-duplex) per carrier

LTE-A throughput
- 1 carrier of MIMO 8x8 DL, 8x8 UL, 20 MHz
- 800 Mbps peak data rate DL
- 400 Mbps peak data rate UL MU-MIMO

Audio transcoding
- 1900+ sessions of G.711 <> G.729
- 1200+ sessions of G.711 <> AMR-NB
- 500+ sessions of G.711 <> OPUS

OCT3032 hardware description

The OCT3032 comprises up to 32 Opus3 DSP cores, a wireless accelerator group, a CPU complex, a total of 18MB of internal memory, and various peripheral interfaces. Its Crossbar Interconnect (XBC) provides a 90 Gbps high-bandwidth interconnect between the DSP cores, CPU complex, peripherals, and external memory.
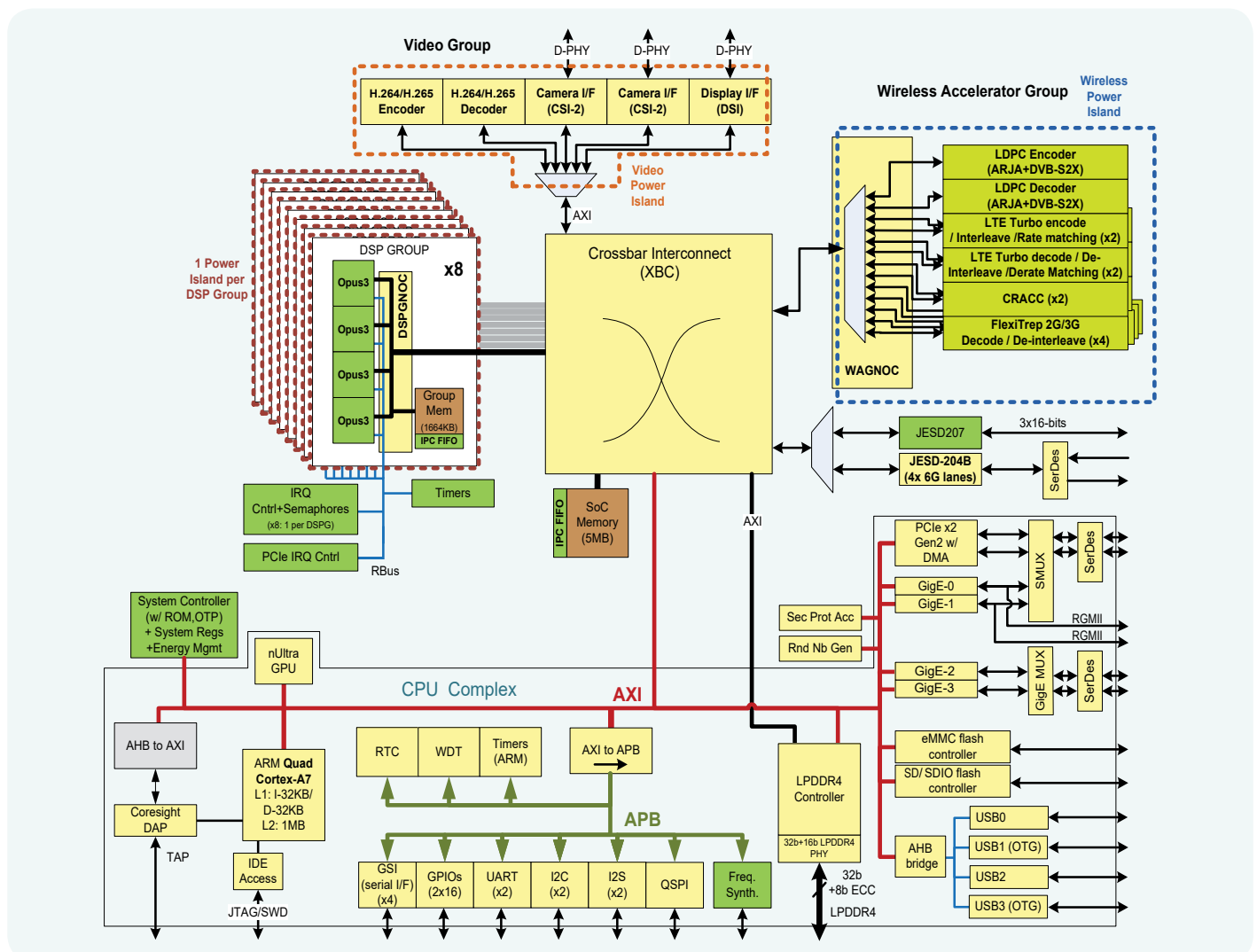
Opus3 DSP core technology

Opus3 is Octasic's third generation of low-power, self-clocking, high-performance DSP core technology. Each Opus3 core offers the following features:

- **Harvard memory architecture**
    - 64kB data L1 cache (2-way associative)
    - 64kB instruction L1 cache (2-way associative)
    - 16kB shared TCM
    - L1 cache memory can be configured as local (TCM) memory

- **32-bit word instructions and scalar processing**

- **128-bit vector processing through its Core-Integrated Hardware Accelerator (CIHA)**

Package description

900-pin Flip Chip Ball Grid Array (FCBGA)

Dimensions	25mm x 25mm x 0.8mm pitch
Power consumption	0.5W to 8W, depending on application

Development tools

Opus Studio, Octasic's integrated development environment (IDE), offers a complete set of development tools for the OCT3032 devices. Opus Studio provides all necessary tools for code editing, compiling, simulation, debugging, and profiling. Octasic also provides a real-time kernel and RTOS services that can be used to rapidly develop embedded applications.

Evaluation and development platform

Octasic offers the OctNode0 platform, from its OCT3032-based OctNode family of boards, for evaluation of the OCT3032 and to expedite application development.

OctNode0 is a frequency-agile, multi-standard small cell platform that integrates one OCT3032 and two RF transceivers. It runs any combination of Octasic's flexiPHY software suite, offering GSM / CDMA2000 / 3G / LTE / 5G capabilities for base station or GSM / LTE for UE.

OctNode0 also supports Octasic's Vocallo media gateway software, a complete solution for audio and video processing over IP and TDM. Vocallo offers a wide selection of codecs, voice quality enhancement, echo cancellation, and media processing features, along with a complete network protocol stack.

To get more information about the OCT3032 SoC and the OctNode0 evaluation and development platform, please contact **sales@octasic.com**