SYNOPSYS®

DesignWare IP for Automotive SoCs

Overview

Synopsys IP and prototyping solutions provide the fastest path from proof-of-concept to verified SoC for automotive applications. Synopsys DesignWare® IP solutions are used to ensure high quality and reliability in applications from infotainment with vehicle connectivity, advanced driver assistance systems (ADAS), gateways, and mainstream microcontrollers (MCUs). In addition, DesignWare IP enables automotive SoC designers to implement the latest protocols required in new applications such as embedded vision, sensor fusion, and cloud connectivity user interfaces. Synopsys' stringent quality and reliability standards give automotive SoC designers confidence when developing their complex SoCs using the latest interface IP, processors, embedded memories and logic libraries in mainstream and advanced process nodes. The ISO 9001 certified Quality Management System for DesignWare IP implements applicable clauses of the IATF 16949 standard supporting additional stringent automotive quality requirements.

Advanced Driver Assistance Systems

ADAS is experiencing rapid adoption and growth in automotive systems enabled by advancements in the underlying driver assistance and autonomous vehicle technologies. Fueled by consumer interest and government regulations focused on improving road safety, auto makers are requiring semiconductor suppliers to implement new capabilities for safety-critical applications such as pedestrian detection/avoidance, lane departure warnings and correction, traffic sign recognition, surround view, drowsiness monitor, and others.

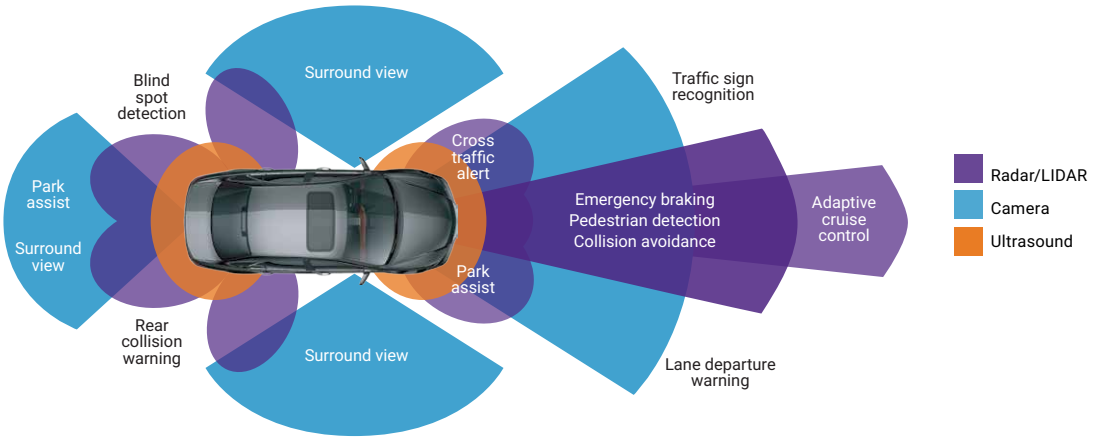

Figure 1: ADAS applications

Benefits of Synopsys DesignWare IP for ADAS

- Industry's widest selection of interface IP, including LPDDR5/4/4X, Ethernet AVB/TSN, PCI Express, CCIX, MIPI, and HDMI, offers high quality and reliability for driver assistance systems
- ARC EV7xFS vision processors support recurrent neural network (RNN) and convolutional neural network (CNN) algorithms while supporting ASIL B or D operations
- ARC Functional Safety Processors deliver pre-built, verified dual-core lockstep cores with integrated safety monitors, supporting ASIL D or B operations and the ISO 26262 automotive safety standard
- Sensor and Control IP Subsystem simplifies the addition of sensor fusion functions
- Security IP for cryptography and protocol acceleration offer platform security and secure boot

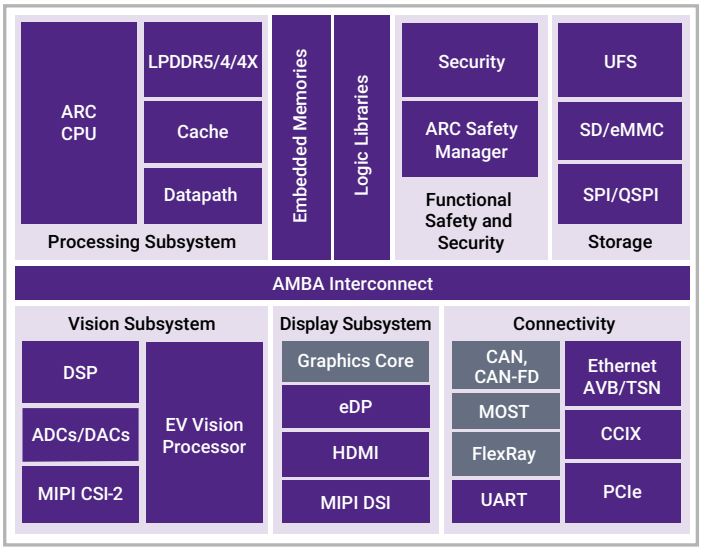

Figure 2: IP for ADAS SoCs

ISO 26262 Functional Safety

Semiconductor suppliers must develop ADAS SoCs and modules in compliance with the ISO 26262 Functional Safety standard. Safety-critical applications rely on SoCs to meet Automotive Safety and Integrity Levels (ASILs) specific to each application. Compliance to the standard also applies to the IP that is integrated into the SoC.

Benefits of Synopsys DesignWare IP for Functional Safety

- Synopsys "safety culture" implements policies, processes, strategies and safety managers (Semiconductor Automotive Functional Professional (SC-AFSP) certified) for safety-related IP development
- Enhanced safety features such as datapath protection, configuration register parity and ECC to memories
- IP delivered with ISO 26262 safety package
- Certified compliant by SGS-TUV Saar
- To see Synopsys' broad portfolio of ASIL Ready ISO 26262 certified DesignWare IP, visit synopsys.com

Connected Vehicle and Infotainment

Auto makers are planning the next-generation passenger experience to embrace the content explosion brought by smartphones and cloud connectivity. From embedded functions such as on-board navigation and satellite radio, to gesture recognition and Internet apps, growth in infotainment with vehicle connectivity is driving the need for flexible and adaptable solutions.

Benefits of Synopsys DesignWare IP for Connected Vehicle and Infotainment

- Multiple interfaces including LPDDR4, PCI Express, USB, DisplayPort, HDMI, MIPI, Ethernet with Time Sensitive Networking (TSN)
- High-Performance Core (HPC) Design Kit with embedded memories and logic libraries ensures the highest performance for CPUs and DSPs
- Security IP for HDCP 2.3 and DTCP-IP increases content protection

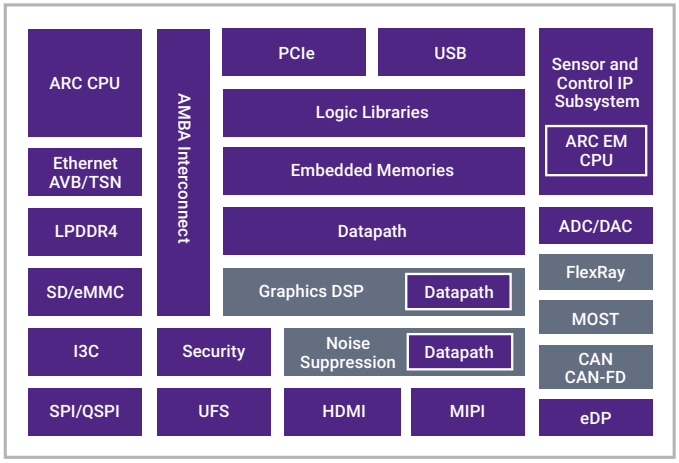

Figure 3: IP for connected vehicle and infotainment SoCs

Gateways

Gateway SoCs for automotive networks manage the system connectivity for domains applications. Due to the increased network bandwidth required by distributed sensors and centralized domain compute processing, automotive gateway SoCs are quickly integrating high bandwidth automotive ethernet Time Sensitive Networking (TSN), using the data prioritization and policy capabilities of Ethernet TSN, to perform advanced network processing. Providing data traffic routing and management, as well as protocol translation, automotive gateway SoCs perform critical system management. The system security, firewall, and intrusion detection operation of the gateway enables secure Over-the-Air (OTA) software management so various domain functions can be updated on an ongoing basis, enabling new services, applications, and use cases. Synopsys offers a portfolio of silicon-proven IP including up to 10G Ethernet IP supporting Audio Video Bridging (AVB) and TSN specifications for real-time data connectivity, ARC processors with ASIL D safety capabilities for real-time data management, and security IP with root of trust for encryption/decryption.

Benefits of Synopsys DesignWare IP for Gateways

- 1Gb and 10Gb Ethernet TSN IP enable data prioritization and data policy protocols
- Security IP provides key management, encryption/decryption, and root of trust
- High performance ARC functional safety processors with ASIL D safety capability provides real-time data management

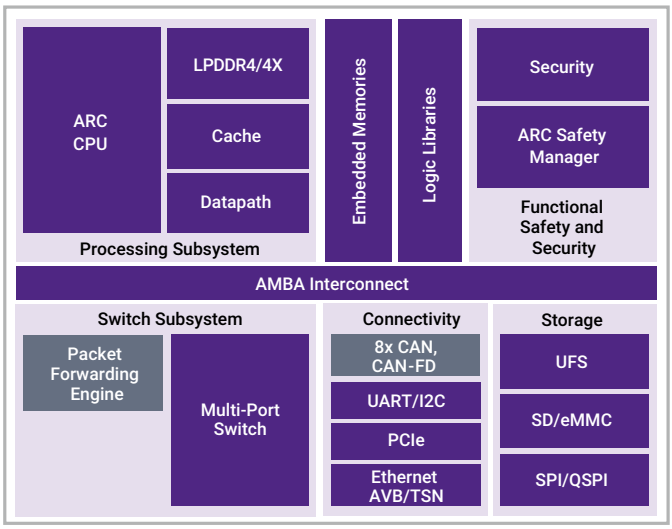

Figure 4: IP for automotive gateways

Mainstream MCUs

Typical new cars contain more than one hundred MCUs throughout the automotive platform. Engine control, body and chassis control, electric vehicle (EV)/hybrid electric vehicle (HEV) battery management, instrument clusters, on-board diagnostics, and other applications continue to expand the requirements for automotive MCUs. In addition, the growth of non-optical and image sensors that monitor engine performance, stabilization, and climate control are driving the addition of sensor fusion capabilities to the MCUs.

Benefits of Synopsys DesignWare IP for MCUs

- Industry's broadest portfolio of interface IP, data converters, high-performance datapath elements, embedded memories and logic libraries, and ARC® functional safety processors and processor-based subsystems
- Sensor and Control IP Subsystem processes data from digital and analog sensors to offload host processors, enabling more power efficient processing of the sensor data
- ARC EM 22FS processor as the safety manager for ISO 26262 safety-compliant automotive applications

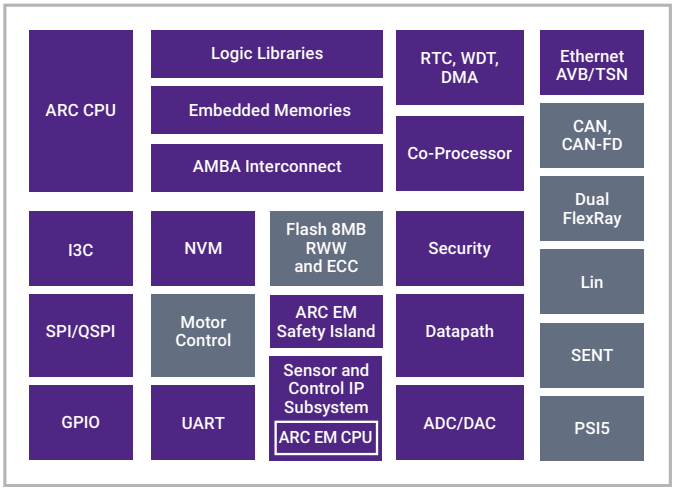

Figure 5: IP for automotive MCUs

Designed for Automotive Reliability

Synopsys DesignWare IP has been designed and tested in accordance to Synopsys' stringent automotive mission profile following automotive-specific design rules. Synopsys verifies our physical IP with very high-reliability automotive Parts Per Million (PPM) targets and critical specifications according to automotive Process Capability Index (Cpk) distributions.

Faster Time-to-Market

SoCs for ADAS, connected vehicles & infotainment, gateways, and MCUs are growing in complexity as they implement high-performance applications such as vision detection/correction as well as extensive multimedia content. To reduce the overall effort and cost of assembling and integrating IP into an SoC, Synopsys offers DesignWare IP Subsystems following an ISO 9001 quality and ISO 26262 functional safety process for ASIL readiness. The subsystems consist of pre-validated, fully integrated solutions that utilize Synopsys' automotive IP and tools for the specific SoC application. In addition, DesignWare IP Subsystems provide extra functionality and value over simply integrating a PHY and controller, e.g., common register interface between the PHY and controller, debug logic, and more. The Interface IP Subsystems include key protocols for automotive such as DDR, PCIe, USB, MIPI, and Ethernet, as well as multi-protocol subsystems.

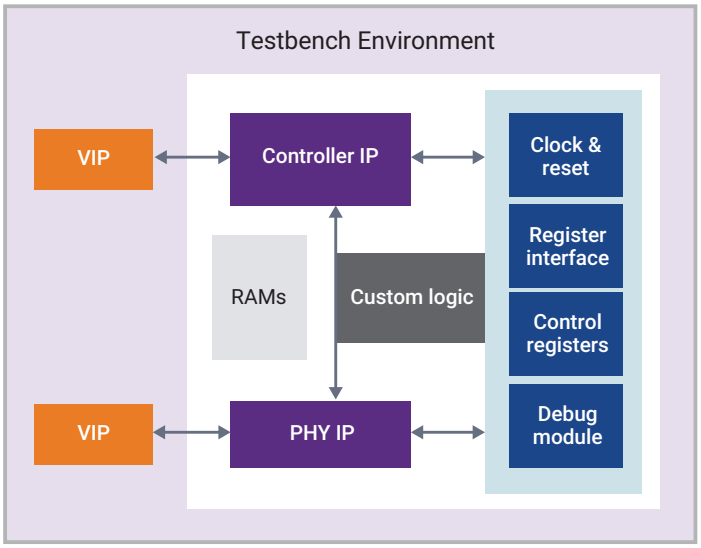

Figure 6a: DesignWare IP Subsystems

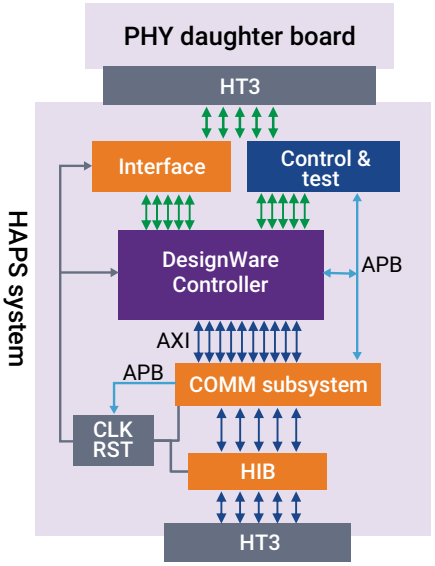

Figure 6b: DesignWare IP Prototyping Kits

DesignWare IP Prototyping Kits include a proven reference design of the target IP pre-tested on a HAPS FPGA-based prototyping system and software development platform running Linux OS. The pre-verified IP configuration can easily be modified to explore design tradeoffs for various automotive applications and offer a quick out of the box IP prototyping experience to accelerate software development.

DesignWare IP	Product Features for Automotive SoCs	Automotive ADAS SoCs Impact
Interface IP		
LPDDR5/4/4X Controller and PHY	Low latency, multi-port memory controller and PHY supporting LPDDR5/4/4X SDRAM speeds up to 6400 Mbps	Multi-port access to shared main memory enables protocol engines for embedded vision and high-performance heterogeneous processing
Ethernet AVB/TSN Controller	10M/100M/1G Ethernet supporting Audio Video Bridging, Time Sensitive Networking, and IEEE-1588 PTP with 1-step time stamping	Independent traffic classes and bounded latency enables precisely synchronized real-time camera and sensor data
MIPI CSI-2 and DSI Host and Device Controllers, MIPI D-PHY	2.5 Gbps per lane interface to image sensors and LCD displays contains flexible CSI-2 and DSI configurations	Enables multiple interoperable camera and display scenarios to support widest range of SoC applications
HDMI Controller and PHY	HDMI IP supporting the latest HDMI 2.1 with HDCP 2.3 specification	Ability to locate ADAS SoC remotely from video system
USB PHY	USB 2.0 and USB 3.0 PHYs are Temperature Grade 2 qualified. USB PHYs operate at USB 3.0/2.0 speeds, interoperable with all USB generations	Enables infotainment SoCs to support next-generation user interfaces with 4K and higher resolution video, imaging, audio and social media applications
PCI Express Controller and PHY	PCIe 3.0 & 4.0 with embedded DMA and debug features supporting endpoint, root port or dual mode operation; choose native or AMBA interfaces to support key automotive processors	Popular chip-to-chip interface to add processor peripherals. Low power L1 sub-states provide lowest power operation
CCIX Controller and PHY	Supports data transfer speeds up to 32Gbps and cache coherency for faster data access	Complex automotive systems with multiple CPUs and accelerators can maintain cache coherency between chips while moving data at high speeds
UFS Host Controller and PHY	Compliant with the latest JEDEC UFS 3.0, MIPI UniPro 1.8, and MIPI M-PHY 4.1 specifications, supports bandwidths up to 23.2 Gbps (2.9 GB/s) when high-speed Gear4 is used, and QoS features allow monitoring and training of the communication channel to enable a reliable link	Addresses the flash storage requirements of both ADAS and infotainment applications by enabling higher capacity, higher bandwidth and lower latency
Processor IP		
32-bit ARC Processor	ARC EM with Safety Enhancement Package (SEP) for ISO 26262 Functional Safety applications with integrated hardware safety features	Optimized for low-power embedded automotive applications, complete solution of processor IP; development tools and safety documentation accelerate development of ASIL D certifiable systems
EV Vision Processor	Lock-step safety island manages functional safety escalation for ADAS SoCs	Fast object detection and recognition for autonomous vehicles, ADAS applications, and in-camera driver detection
Foundation IP		
Embedded Memories	HPC Design Kit optimized for SoC processors: CPU, GPU and DSP; designed for demanding electro migration (EM) conditions; STAR Memory system with EEC support for multi-bit error correction	Enables optimal implementation across all three dimensions: performance, power, and area; SEU mitigation enables highest reliability
Embedded Test and Repair	STAR Memory System integrated test, repair and diagnostic solution for embedded memories. STAR Hierarchical System for automated hierarchical test for all IP and logic blocks on an SoC	Achieve low DPPM for designs needing up to ASIL D. Field algorithmic programmability and mission mode testing improve reliability for functional safety applications
NVM	AEC Q100 Temperature Grade 0 qualified NVM replaces eFuses for calibration and trimming applications; Synopsys portfolio includes multi-time programmable and one-time programmable NVM	Ideal for sensors, power management, LCD controllers, and precision analog
Analog IP		
12-bit SAR ADC	High resolution up to 12-bit, 320MSPS ADC/DAC converters; high dynamic range and high speed for extended application range; compatible with embedded flash	Integrated ADC reduces system form factor and extends application range for fast moving signal processing for multimedia and ADAS
Security IP		
Security IP	Broad array of content protection IP, hardware cryptographic engines and middleware, and embedded security modules with tRoot Secure Hardware Root of Trust for identification and authentication	Complete security IP portfolio helps prevent a wide range of evolving threats in connected cars such as theft, tampering, side channel attacks, malware and data breaches
IP Subsystem		
Sensor & Control IP Subsystem	Optimized to process data from digital and analog sensors. Offload host processors to enable more power-efficient processing of the sensor data; implemented using Synopsys' 32-bit ARC EM processor with ASIL D ISO 26262 Functional Safety Package	Reduces cost, complexity and development effort by pre-integrating sensor and actuator-specific IP blocks together with software in a single subsystem; enables sensor fusion by consolidating multiple sensor inputs to the SoC

For more information on DesignWare IP for automotive applications, visit synopsys.com/ip-automotive.

SYNOPSYS®
Silicon to Software™

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