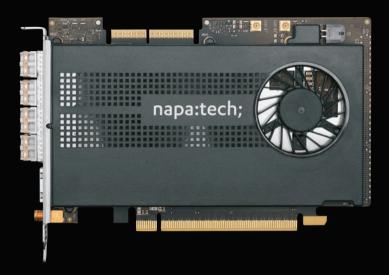


NT100A01 SmartNIC with Link[™] Capture Software

4×1/10G, 4×10/25G

DATA SHEET



Packet Capture and Replay

Use cutting-edge SmartNIC technology to add real-time line-rate performance to your application. The NT100A01 SmartNIC provides full packet capture of network data at 100 Gbps with zero packet loss. Nanosecond precision time-stamping and merge of packets from multiple ports ensures correct timing and sequencing of packets. The NT100A01 SmartNIC can also be used for 100% packet replay with nanosecond precision of all networking traffic for analytics, testing and simulation.

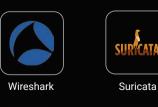
The NT100A01 SmartNIC enables full utilization of CPU cores through advanced receive side scaling with support for tunneling protocols, such as GTP, IP-in-IP, NVGRE and VxLAN. The NT100A01 SmartNIC can also remove duplicate packets, slice packets and filter packets to reduce the amount of data and thereby offload the server system and applications. Stateful flow processing with support for up to 50 million flows enables CPU-hungry applications, such as Suricata, to intelligently select exactly which flows to process and which to ignore. Flow records are maintained for all flows and reported to the application.

The NT100A01 SmartNIC also comes in a NEBS level 3 compliant variant.

Applications

Napatech SmartNICs enable implementation of highperformance network appliances based on standard servers. Examples of applications include:

- Quality of experience optimization
- Financial latency measurement
- Customer experience analysis
- Data loss prevention
- Cyber defense
- · Fraud detection and compliance management
- · Infrastructure management and security
- Network and application performance
- Troubleshooting and compliance







ntop

n2disk



Zeek



Snort

TRex

FEATURE HIGHLIGHTS AND SPECIFICATIONS

Rx Packet Processing

- Zero packet loss for packet size 64 10,000 bytes
- Sustained traffic up to 100 Gbps
- Line rate 4 x 25 Gbps traffic burst, 680 milliseconds buffering
- Multi-port packet merge, sequenced in time stamp order
- L2, L3 and L4 protocol classification
- L2 and L3/L4 (IP/TCP/UDP) checksum verification
- GTP, IP-in-IP, GRE, NVGRE, VxLAN, Pseudowire, Fabric Path, VNtag tunneling support
- Pattern match, network port, protocol, length, and error filters
- · Custom flow definitions based on 2-, 3-, 4-, 5- or 6-tuple
- Flow match/actions: Forward to application or network port or drop packet
- Stateful flow management
 - Up to 50 million bidirectional IPv4 or IPv6 flows
 - Learning rate: 2 million flows/sec
 - · TCP flow termination, flow timeout, or application-requested
 - Flow records with Rx packet/byte counters and TCP flags
- Stateless flow management
- Up to 36,000 IPv4 or up to 7,500 IPv6 2-tuple flows
- Custom hash keys, symmetric hash key option
- · CPU load distribution based on hash key or filter or per flow
- 128 Rx queues, 16 MB 1 TB Rx buffer size
- · Packet descriptors with metadata
- IP fragment handling
- Deduplication
- · Slicing at dynamic offset or fixed offset from start or end of packet
- Header stripping, protocol layers between outer L2 and inner L3 $(\ensuremath{^*})$
- Packet masking, 1 64 bytes at dynamic or fixed offset (*)
- Extended RMON1 and counters per filter and per queue

Tx Packet Processing

- Line rate Tx up to 100 Gbps for packet size 64 10,000 bytes
- Replay as captured with nanoseconds precision
- Per-port traffic shaping
- Port-to-port forwarding
- L2 and L3/L4 (IP/TCP/UDP) checksum generation
- 128 Tx queues, 4 MB Tx buffer size

Time Stamping and Synchronization

- Rx time stamp and Tx time stamp inject
- OS time, PPS and IEEE 1588-2008 PTP V2 synchronization
- Synchronization between SmartNICs
- Time stamp formats: Unix 10 ns, Unix 1 ns, PCAP 1 us, PCAP 1 ns

Network Standards

· IEEE 802.3 1G, 10G and 25G Ethernet

Supported pluggable modules

- 1000BASE-T, SX, LX, ZX
- 10GBASE-SR, CR, LR, ER
- 25GBASE-SR, LR, LR-BiDi

(*) Future release

Software

- Operating systems: Linux and Windows
- libpcap, WinPcap and DPDK
- Napatech NTAPI for highest performance and advanced features
- SDK tools included in source code for debugging and prototyping and as application examples

Hardware

- Xilinx XCVU5P FPGA
- 8 GB DDR4 SDRAM
- PCIe Gen3 16 lanes @ 8 GT/s
- 4 × SFP28 network ports
- RJ45-F 100/1000BASE-T IEEE1588 PTP
- SMA-F PPS input/output
- 2 × internal MCX-F PPS and NT-TS time sync
- Stratum-3E-compliant TCXO
- · Flash memory with support for two boot images
- Built-in thermal protection
- Physical dimensions: 1/2-length and full-height PCIe
- · Weight excluding pluggable modules:
 - NT100A01-SCC: 355 g
- NT100A01-NEBS: 350 g
- MTBF according to UTE C 80-810:
 - NT100A01-SCC: 317,821 hours
- NT100A01-NEBS: 398,565 hours
- Power consumption including 100GBASE-SR4 modules and typical traffic load:
- NT100A01-SCC: 44 Watts
- NT100A01-NEBS: 44 Watts

Environment for NT100A01-SCC

- Operating temperature: 0 °C to 45 °C (32 °F to 113 °F)
- Operating humidity: 20% to 80%

Environment for NT100A01-NEBS

- Operating temperature: –5 °C to 55 °C (23 °F to 131 °F) measured around the SmartNIC
- Operating humidity: 5% to 85%
- Altitude: < 1,800 m
- Airflow: >= 2.5 m/s

Regulatory Approvals and Compliances

 PCI-SIG[®], NEBS level 3, CE, CB, RoHS, REACH, cURus (UL), FCC, ICES, VCCI, RCM

Orderable port speed configurations

Product	Data Rates included
NT100A01-4×25/10/4×10/1	$4\times10/25~\text{Gbps}$ and $4\times1/10~\text{Gbps}$
NT100A01-4×10/1	4 × 1/10 Gbps

NAPATECH.COM

Also avaible in NEBS variants.

NAPATECH RECONFIGURABLE COMPUTING

Disclaimer: This document is intended for informational purposes only. Any information herein is believed to be reliable. However, Napatech assumes no responsibility for the accuracy of the information. Napatech reserves the right to change the document and the products described without notice. Napatech and the authors disclaim any and all liabilities. Napatech is a trademark used under license by Napatech A/S. All other logos, trademarks and service marks are the property of the respective third parties. Copyright © Napatech A/S 2021. All rights reserved.